ITSS
24th International Travelling Summer School on Microwaves and Lightwaves
5-11 July 2014, Copenhagen, Denmark

GOETHE UNIVERSITÄT FRANKFURT AM MAIN

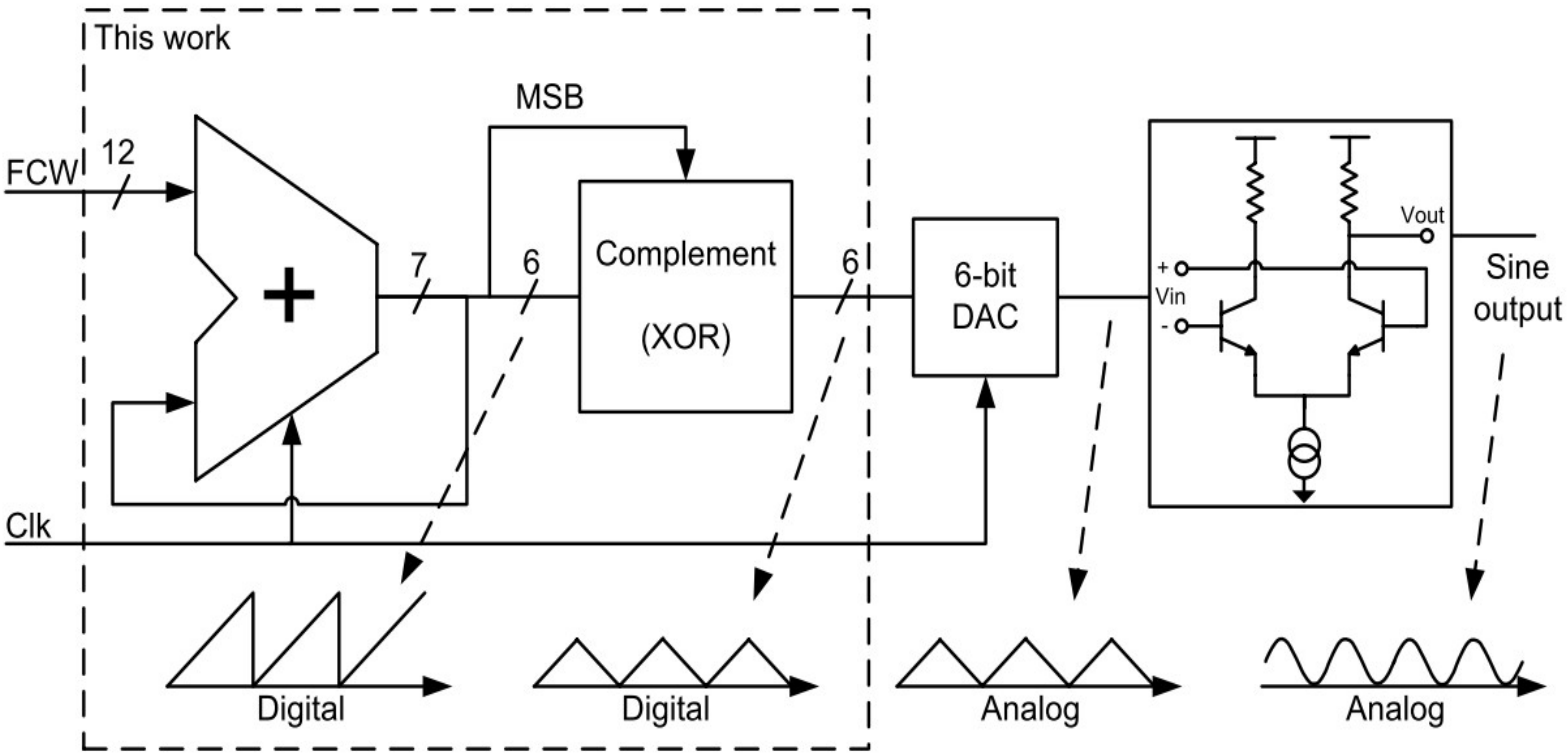
High Speed 12-bit Arbitrary Waveform Generator (AWG)

André Ehlert
Ph.D.-Student

Terahertz Photonics – Institute of Physics
Goethe University Frankfurt am Main

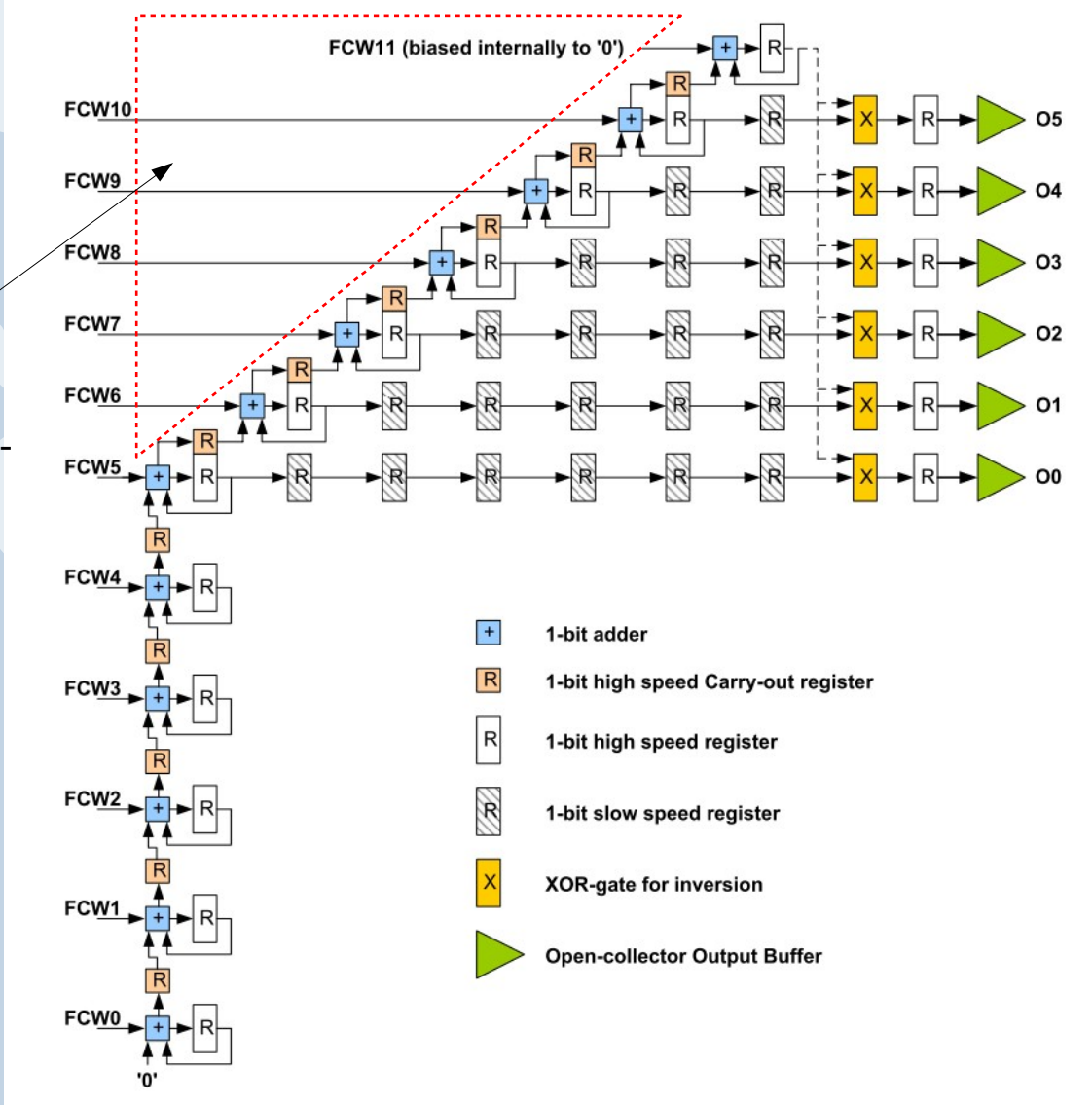
Previous Work – Initial Point

Block diagram of the DDS



Main Part – The Accumulator

Omitted pre-skew registers lead to a phase-shift when switching the FCW



Goals

Enhancement of the accumulator

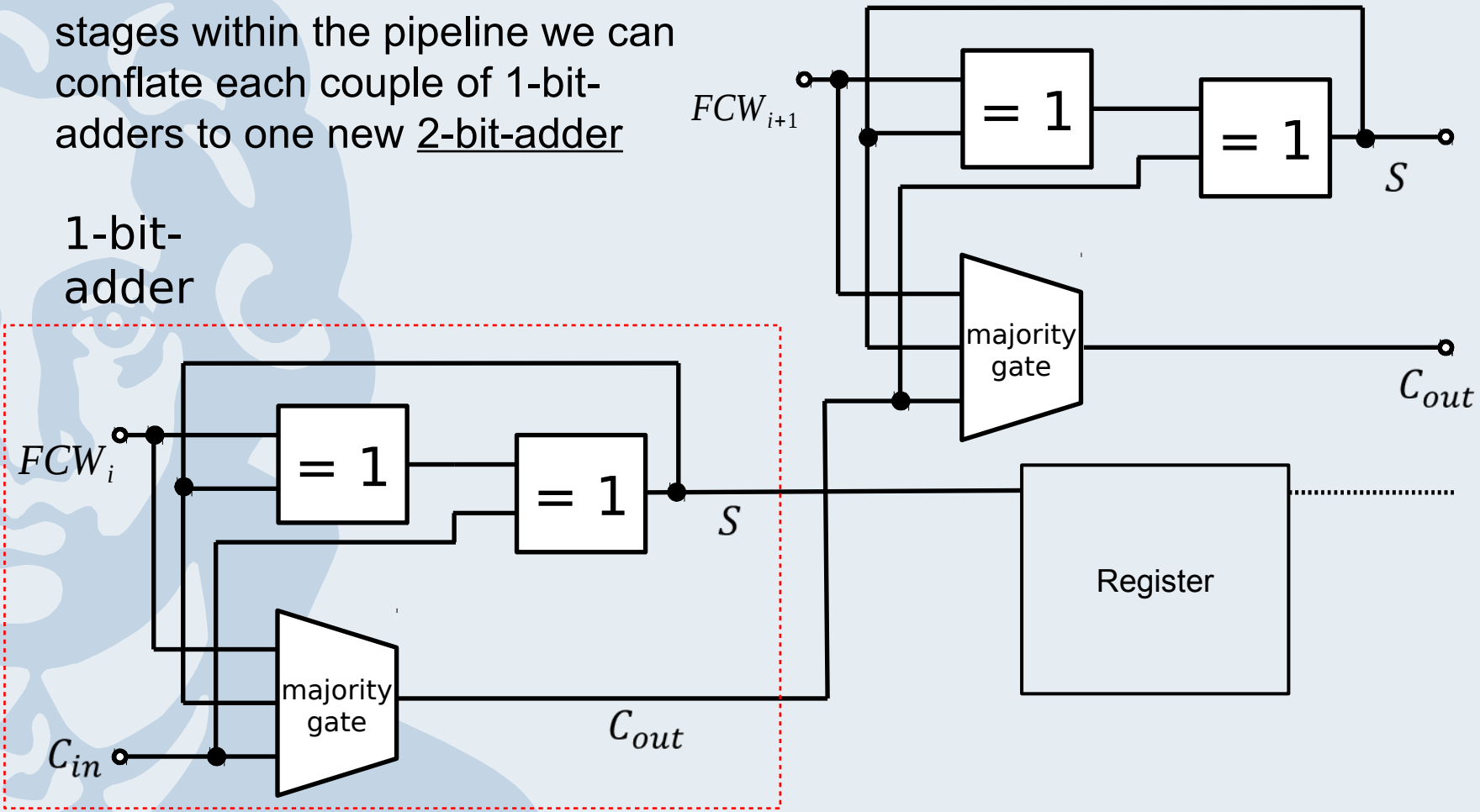
- Reduction of the power consumption (currently: ~1W)
- Providing a **P**hase **C**ontrol ***W***ord (PCW) makes it possible to manipulate the phase of the output signal while the system is running
- Secondary: increasing the clock frequency (currently: 20GHz)

Bringing together the accumulator and the DAC on one chip

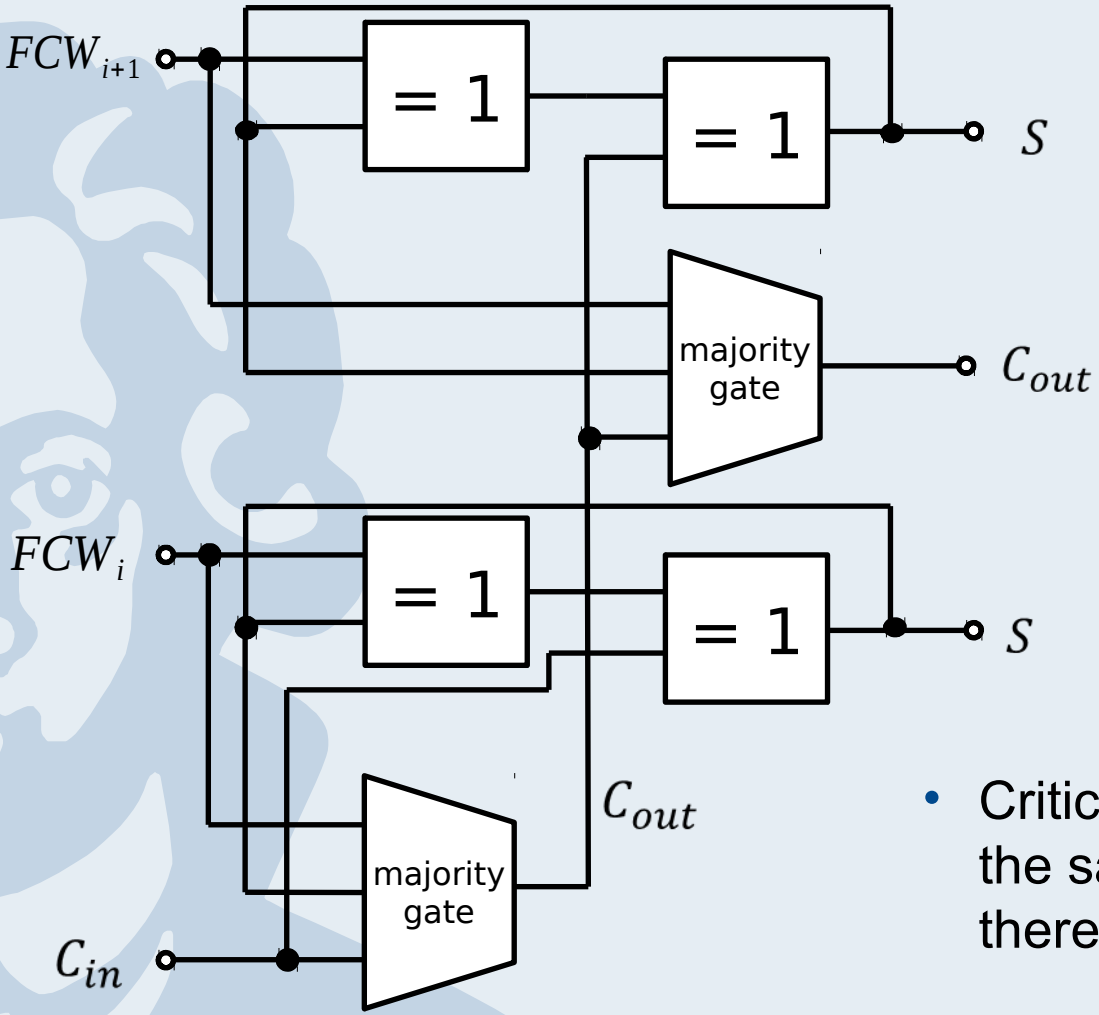
- IHP from Frankfurt (Oder) provides a 6-bit DAC that can be used as a „black box“
- In the previous work the accumulator was a separate chip

Current State - Accumulator

- In order to reduce the number of stages within the pipeline we can conflate each couple of 1-bit-adders to one new 2-bit-adder



Current State - Accumulator

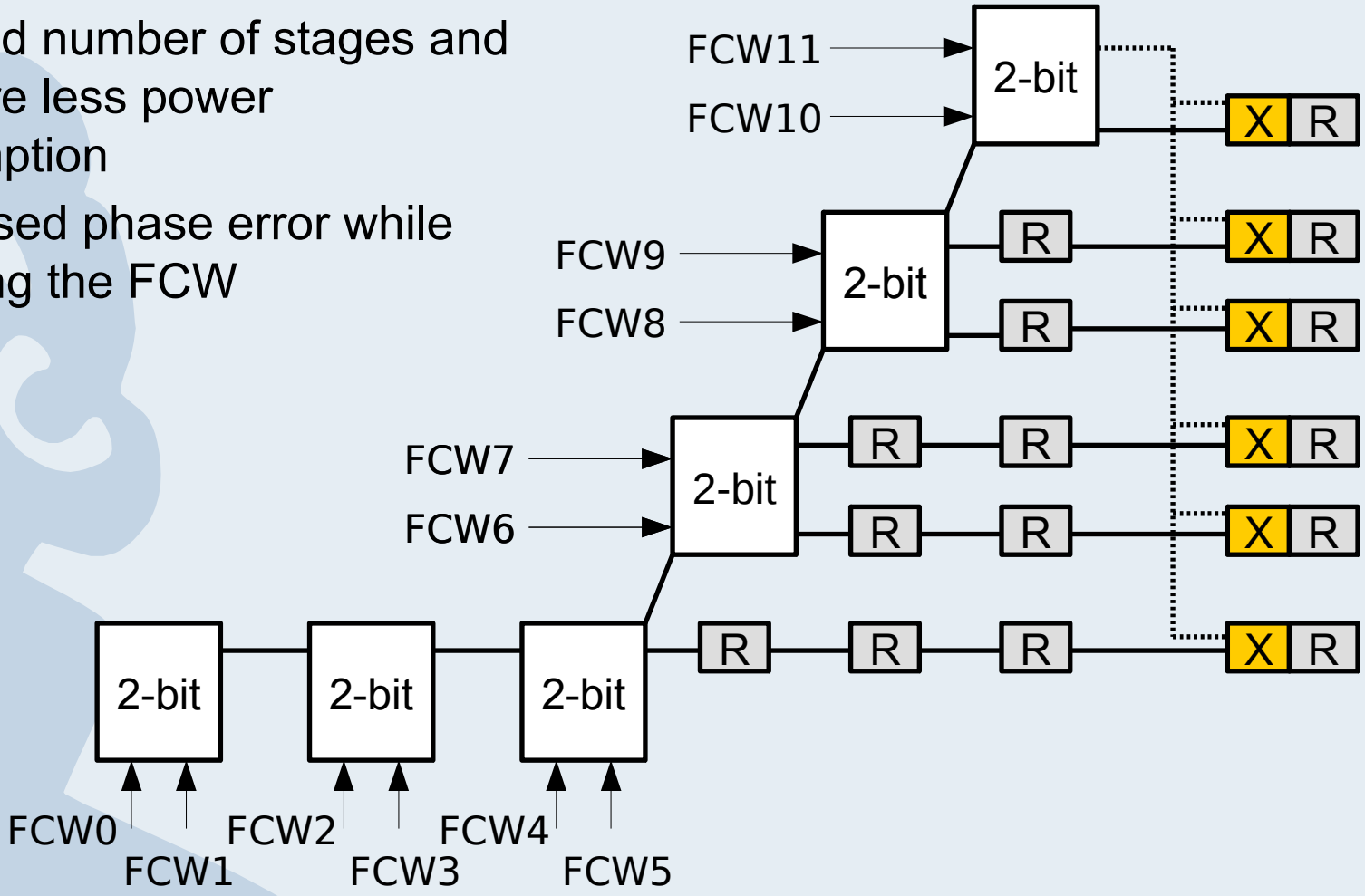


2-bit-adder

- Critical path length remains the same (2 gates), thus there's no loss in speed

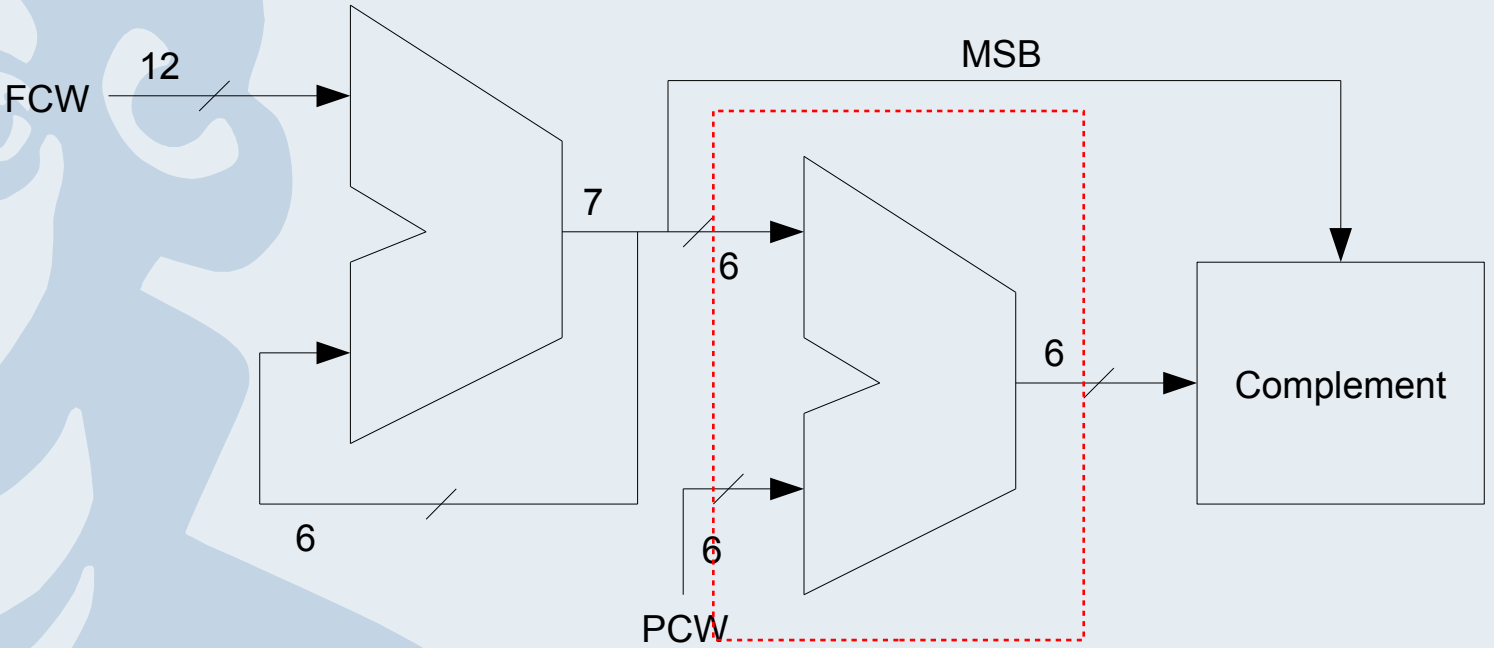
Current State - Accumulator

- Reduced number of stages and therefore less power consumption
- Decreased phase error while switching the FCW



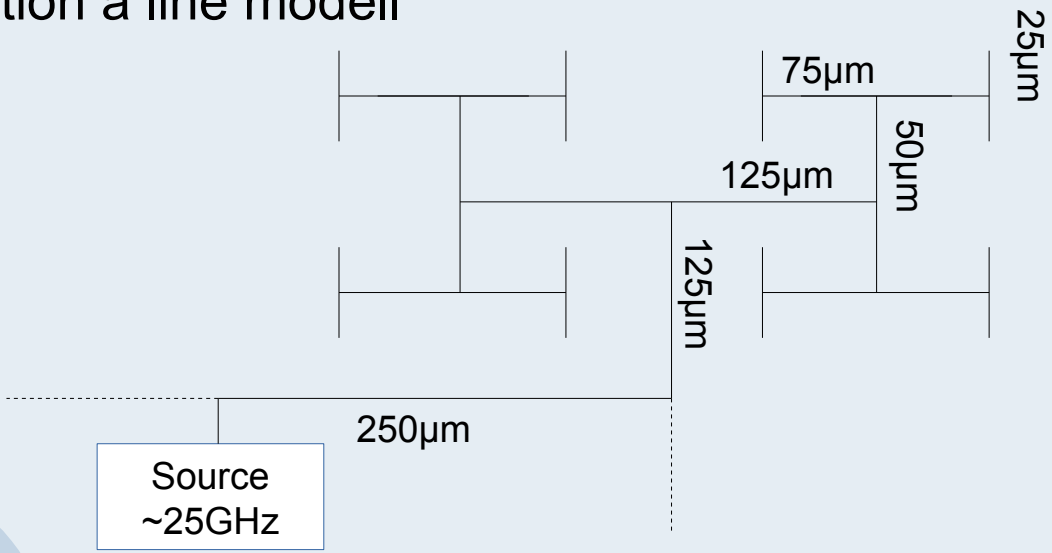
Current State - Accumulator

- In order to provide a PCW, it's necessary to include further adders within the DDS
- This way the DDS becomes an **A**rbitrary **W**aveform **G**enerator (AWG)



Current State - Accumulator

- Further important issue: clock distribution
- At high frequencies it's necessary to control the clock screw very carefully
- Therefore a H-Tree structure is used to ensure that the signal path length from the clock source to each gate is exactly the same
- Layout is finished, but not simulated yet
- For a realistic simulation a line modell will be used



Future Plans

- Clock source shell be integrated on the chip:
  therefore a VCO (+PLL) is needed to generate a stable clock signal @25-30GHz

- Using another technology to run the chip at higher frequencies
  - Currently: 0.25µm SiGe:C BiCMOS technology with npn-HBTs up to $f_T/f_{max} = 180/220\,GHz$
  - Planned: 0.13µm technology with npn-HBTs up to $f_T/f_{max} = 250/300\,GHz$

Acknowledgement

Prof. Dr.-Ing. Viktor Krozer
Institute of Physics, Goethe University Frankfurt am Main

IHP GmbH
Innovations for High Performance Microelectronics

Thank you for your attention!