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High Efficiency Power Amplifiers for High Frequency Application

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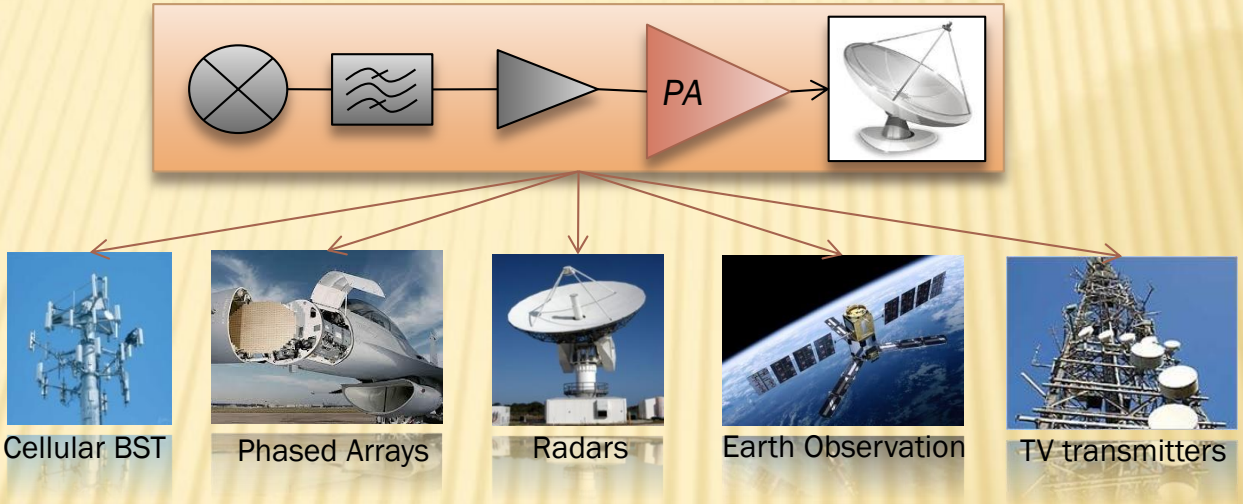
OUTLINE

- Introduction
- Classes of operation
  - Biasing vs. Operating mode
- Design Process
- Simplified design criteria
  - Tuned Load example
- Advanced design criteria for high frequency PA
  - Output Harmonic Tuning
  - Input Harmonic tuning
- Experimental results
  - Class F, 2^{nd} HT, 2^{nd} & 3^{rd} HT
- Conclusions

INTRODUCTION

- Power Amplifiers (PAs) are key elements in TX chain for various applications



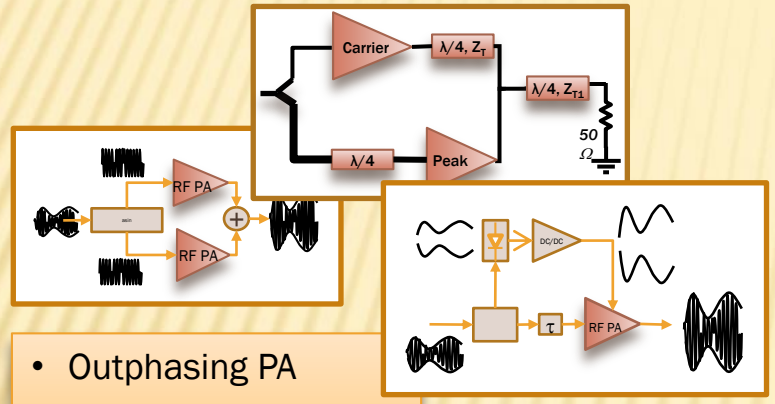
- The aim of a ***PA*** is to increase the power level of signals to be transmitted, without affecting the information content. Different features are required in a PA, depending on the application:
  - integrability and repeatability
  - low voltage operation
  - low dissipated power
  - high output power
  - reliability

→ ***High efficiency PA*** is required!

INTRODUCTION

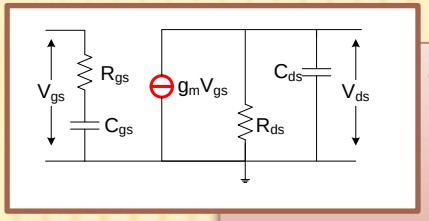
- How can be attained ***high efficiency*** ?

1. Architectural level

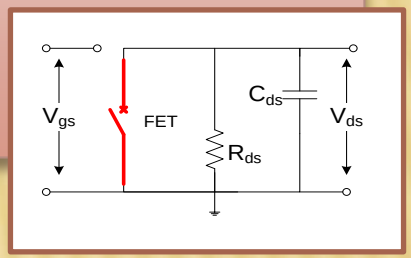


- Outphasing PA
- Envelope Tracking
- EER
- Polar Transmitter
- ***Doherty amplifier***

2. Transistor level



- Current mode:
  - Class F
  - *Harmonic Tuning*
- Switched mode:
  - Class D
  - ***Class E***



- Increase of ***average*** efficiency and linearity

- ***Waveform engineering*** approaches
- Increase of ***absolute peak*** efficiency

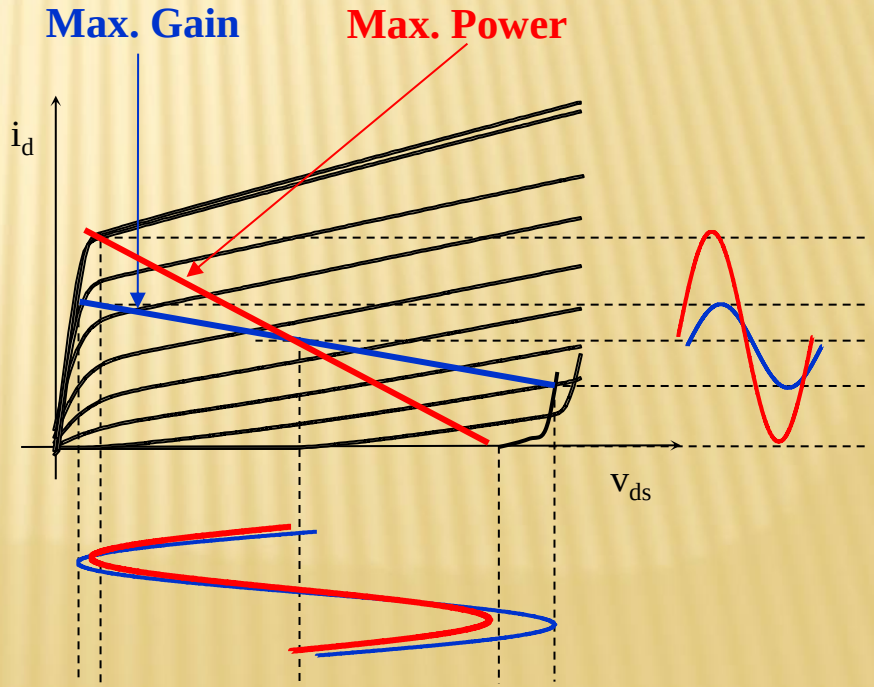
LINEAR VS. NON LINEAR DESIGN APPROACH

- In the case of **Power Stages**, active devices are demanded to deliver a high power level in high linearity conditions, while starting from low levels of power available at the input source.
- The optimal condition is obtained through a conjugate matching at the input and a proper loading at the output, maximizing current and voltage swings, thus allowing maximum output power.
- This gain is named ***power gain***.

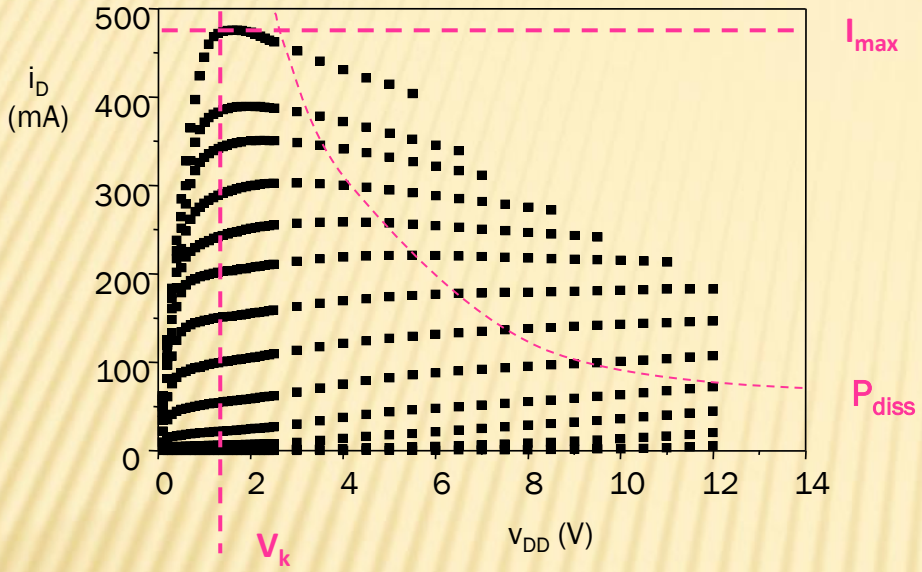
$$\Gamma_S = \Gamma_{in}^*$$

$$\Gamma_L : maxmize(P_{out})$$

Power Match Condition



DEVICE POWER LIMITING MECHANISMS



- The I-V swing limitation ***is not*** frequency related (i.e. device characteristics).
  - Output power level ***is not*** frequency dependent !
  - Power gain ***is*** frequency dependent!

Technological progress improves device physical constraints

- Increases maximum current (I_{max}) and breakdown voltage (V_{br})
- Decreases knee voltage (V_k)
- Increases device thermal disposal (i.e. increases maximum device P_{diss})

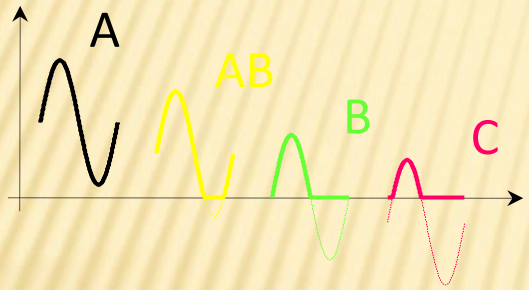
Design strategies are required to attain highest performance from the available devices

- Switched-mode (***Class E***)
- Current-mode (***Class F, HM, …***)
- System architectures (***Doherty, EER, ET,…***)

CLASS OF OPERATION (1/2)

- By such a generic term, a variety of different subjects are indicated.

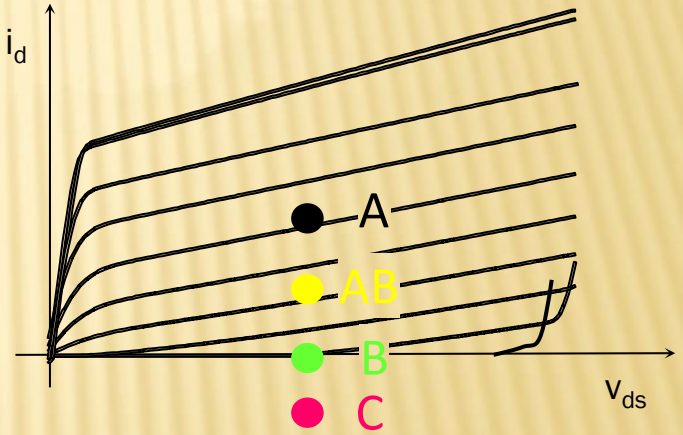
depending on the duty cycle of the device drain (collector) current



biasing class

- class A
- class AB
- class B
- class C

defined through the selected quiescent bias point



$\alpha = 2\cdot\pi$	⇒	Class-A
$\pi < \alpha < 2\cdot\pi$	⇒	Class-AB
$\alpha = \pi$	⇒	Class-B
$\alpha < \pi$	⇒	Class-C

$I_d = I_{max} / 2$	⇒	Class-A
$0 < I_d < I_{max} / 2$	⇒	Class-AB
$I_d = 0$, $V_{gg} = V_{po}$	⇒	Class-B
$I_d = 0$, $V_{gg} < V_{po}$	⇒	Class-C

The duty cycle depends on the quiescent bias point, on the drive level & on the output termination:

not equivalent definitions

CLASS OF OPERATION (2/2)

- With the term ***Class*** can be also indicated

an operating mode
- Class E
- Class D
- …

- The active device is forced to operate as a switch

an harmonic *input/output* tuning strategy
- Tuned Load
- Class F
- …

- The active device acts as a controlled current source (as an amplifier) being loaded at harmonic frequencies by suitable terminations.

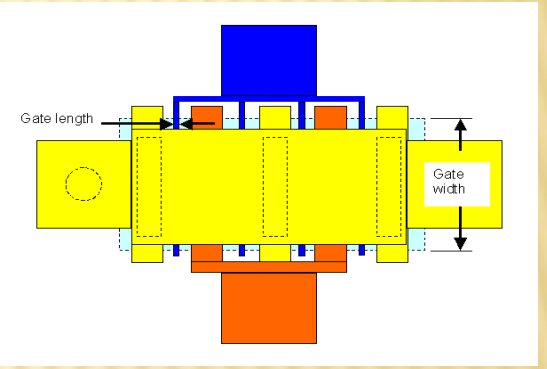
- A given device may be biased in a given biasing class and may adopt an harmonic tuning strategy: for instance, a Class AB - Class F amplifier stage

DESIGN PROCESS

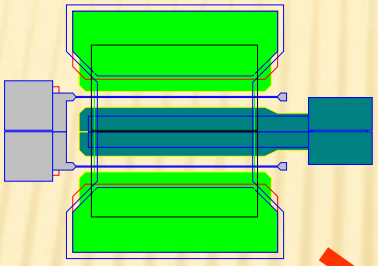
- The design of a power amplifier, as well as any electronic circuit, implies the following steps:
  1. Select device technology and amplifier architecture performing preliminary dimensioning to meet specifications:
     - *device widths,*
     - *no. of stages*
     - *etc.*
  2. Decide DC operating point (bias) for each device/stage
  3. Perform stability analysis over wide frequency range
     - *If required, stabilize the device*
  4. Design matching and DC bias networks to meet required performances
  5. Verify design, test, modify, iterate …
  6. Perform statistical, yield analysis …

DEVICE SCALING

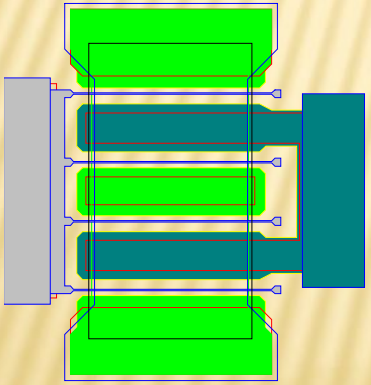
- The dimension of the power devices depends on two parameters:
  - number of fingers and
  - length of the fingers



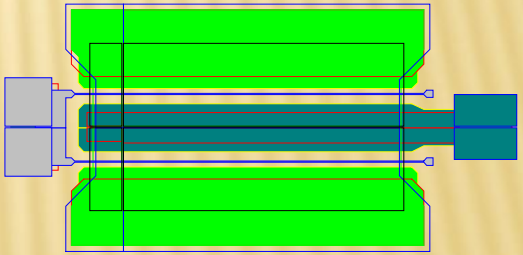
Number of fingers



Length of fingers



Device Scaling

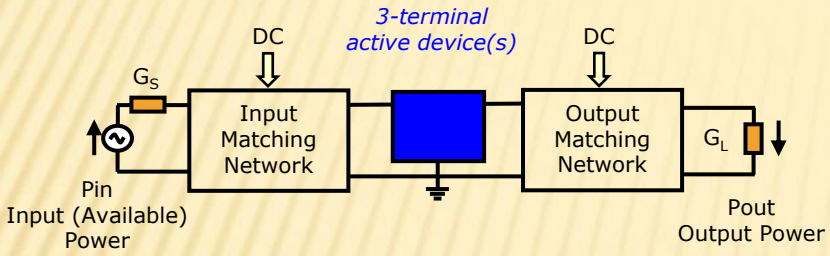


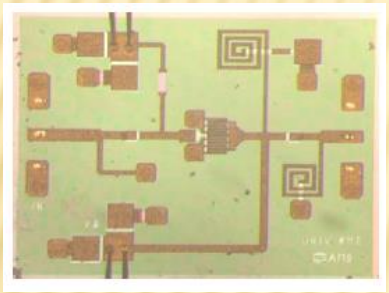
General rule: increasing the dimensions

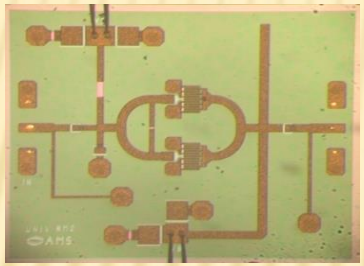
☺ power increases ☹ gain decreases

AMPLIFIER CONFIGURATIONS (1/2)

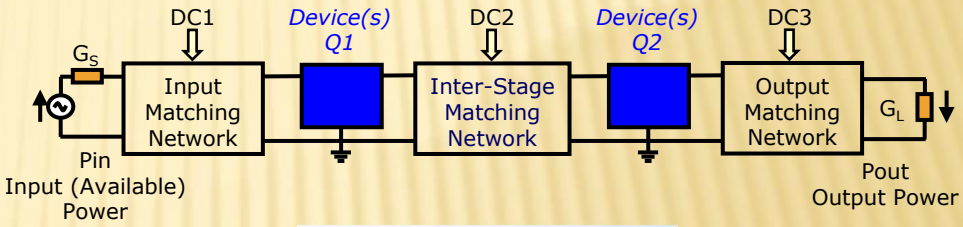
Single-Ended Single-Stage

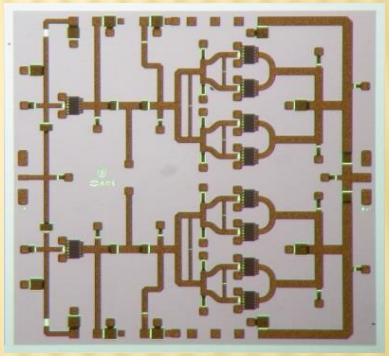






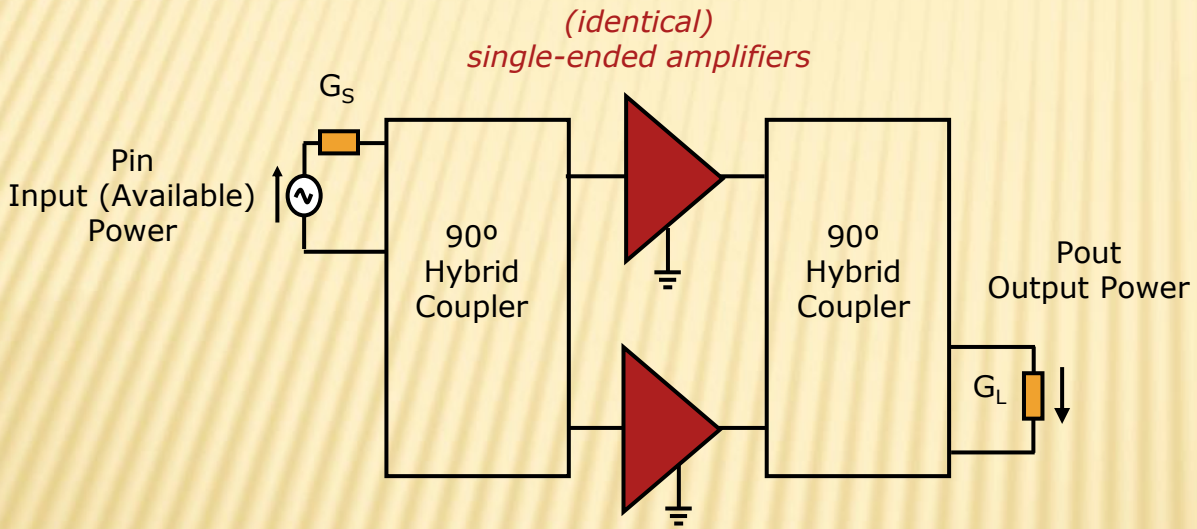
Single-Ended Multi-Stage

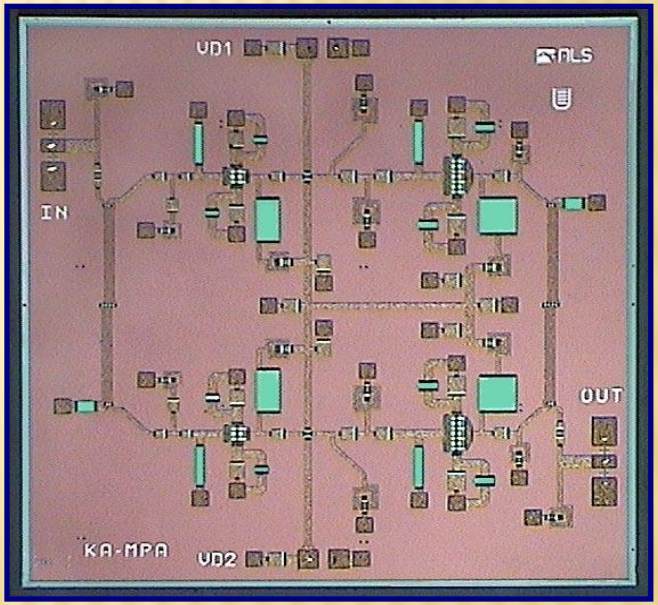




AMPLIFIER CONFIGURATIONS (2/2)

Balanced





POWER BUDGET

- For a given output power and gain (and a chosen technology), the general topology of the amplifier to be designed depends mainly on the power density (W/mm) of the process.

Power Budget Example

Process

- *GaAs* PHEMT
- power density δ_P=630mW/mm

Requirements

- Output power P_{out}=38dBm (6.5W)
- Power Gain > 15dB

Device	W (mm)	Gain G_P (dB)	Gain G_L (dB)
D_1	1	8	10.5
D_2	1.5	7.5	10.0
D_3	2	7	9.5

Pout (mW)	Pout (dBm)
630	28
945	29.7
1260	31

POWER BUDGET

1. Determine the total gate periphery T_G required to obtain 6.5W

$$T_G = \frac{P_{out}}{\delta_P} = \frac{6500}{630} \approx 10.3\ mm$$

2. Determine the correspondent number N of devices

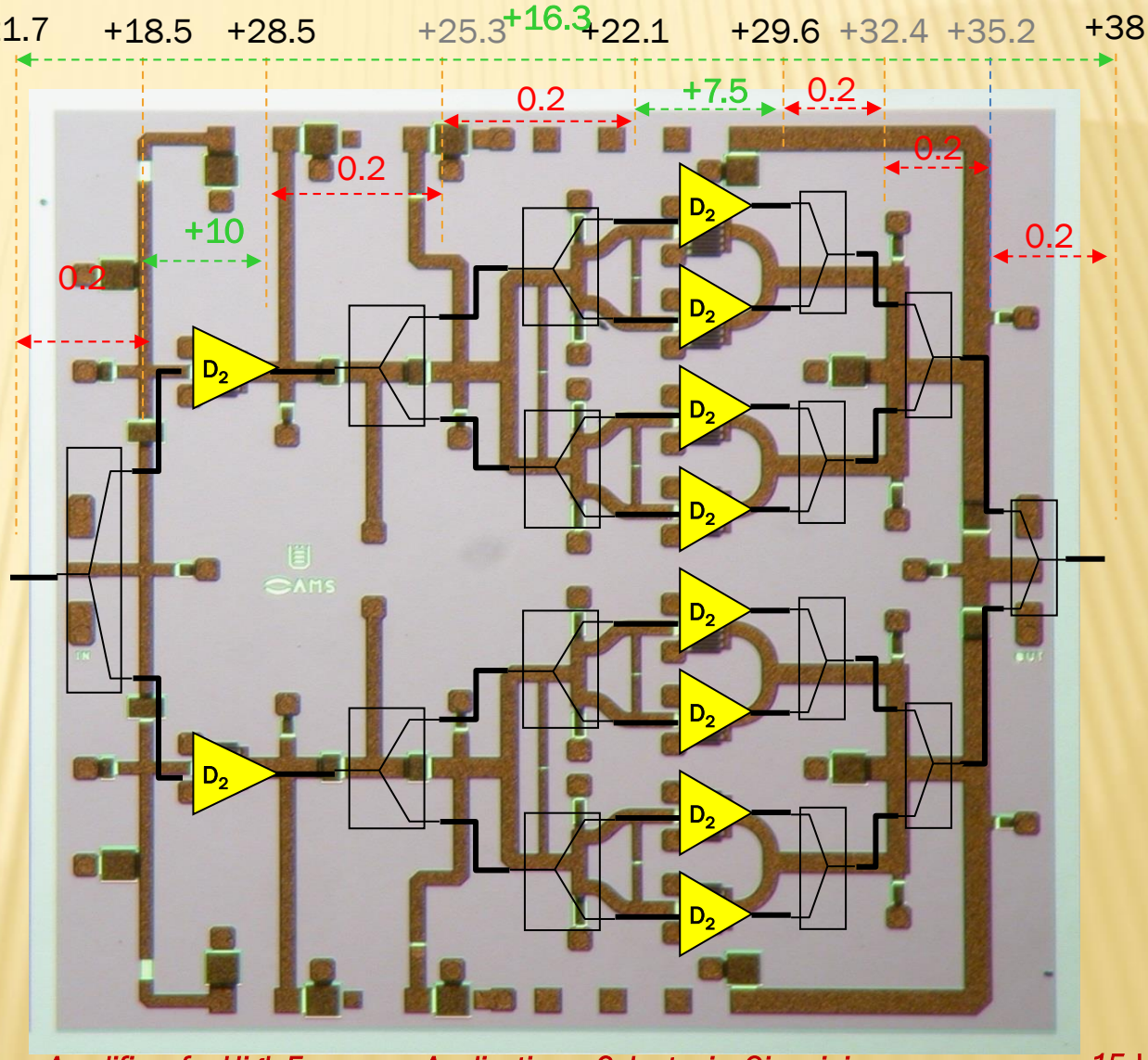
$$N = 2^n > \frac{T_G}{W}$$

Device	W (mm)	N device
D_1	1	16
D_2	1.5	8
D_3	2	8

3. Accounts for network combining losses L.
   In this example, for sake of simplicity, a constant loss has been assumed
   ➔ L=0.2 dB

EXAMPLE

Device	W (mm)	Gain G_P (dB)	Gain G_L (dB)	Pout (mW)	Pout (dBm)
D_1	1	8	10.5	630	28
D_2	1.5	7.5	10.0	945	29.7
D_3	2	7	9.5	1260	31



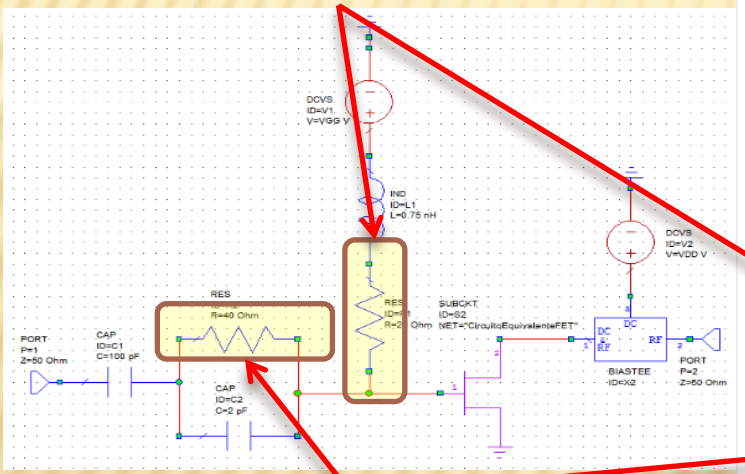
STABILITY ISSUES

- Stability of selected transistors must be guaranteed

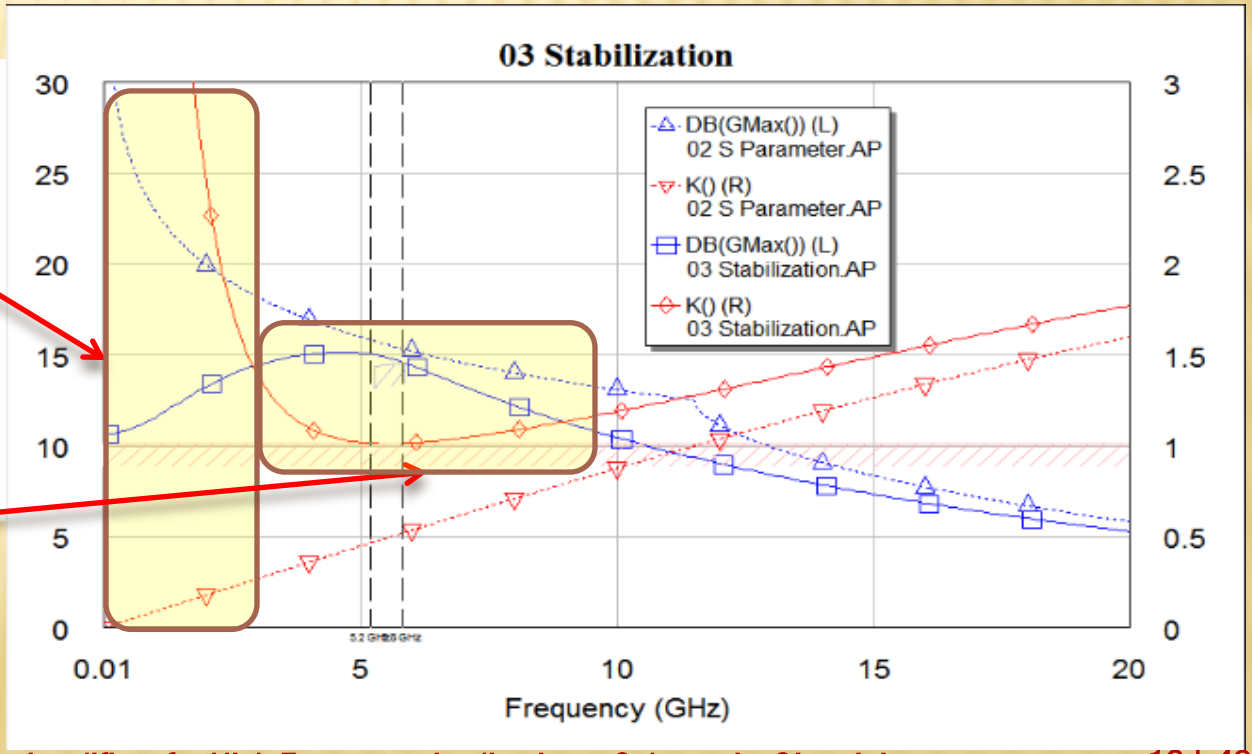
$$K = \frac{1 + |S_{11} \times S_{22} - S_{12} \times S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \times |S_{12} \times S_{21}|}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11} \times S_{22} - S_{12} \times S_{21}|^2$$

Parallel resistance increases low-frequency stability

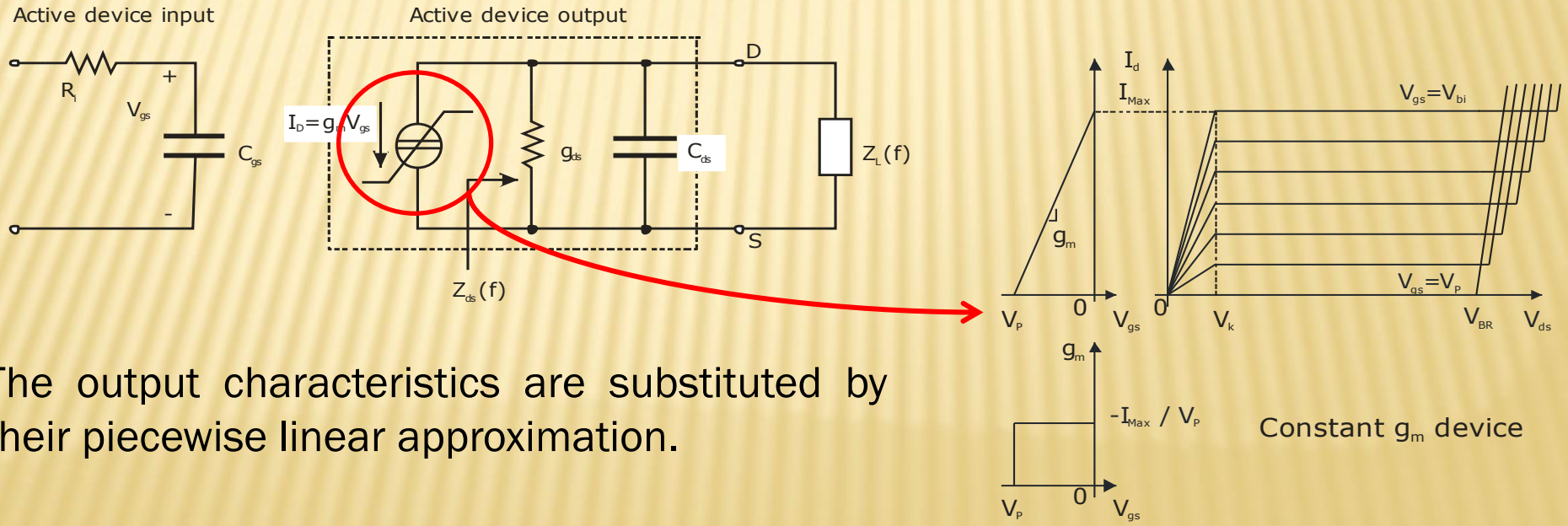


Series resistance increases in-band stability



SIMPLIFIED APPROACH

- A simplified approach can be used to easily infer preliminary device features, if no data (e.g. power density) is provided.
- The active device is modeled through a simplified equivalent circuit, where only the drain-source (FET) or collector-emitter (BJT) controlled current source is assumed to be non linear, and all the parasitic and feedback elements are neglected



- The output characteristics are substituted by their piecewise linear approximation.

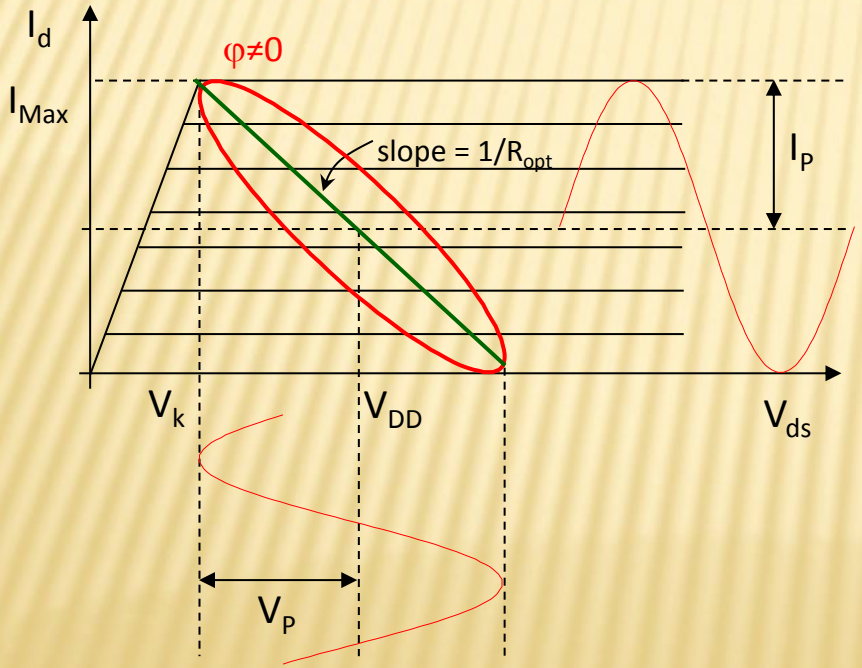
CLASS A

- The output current is driven by the input signal. Assuming a Class A bias condition:
- Assuming a generic intrinsic load impedance Z_{ds}
- The output voltage is related to the output current by means of the intrinsic impedance Z_{ds}

$$i_d(t) = I_p \cdot \cos(\omega t)$$

$$Z_{ds} = |Z_{ds}| \cdot e^{j\varphi}$$

$$v_{ds}(t) = V_p \cdot \cos(\omega t + \varphi) = -|Z_{ds}| \cdot I_P \cdot \cos(\omega t + \varphi)$$



- The output power is given by

$$P_{rf} = \frac{1}{T}\int_0^T p(t)\,dt = \frac{1}{2} I_P \cdot V_p \cdot \cos(\varphi)$$

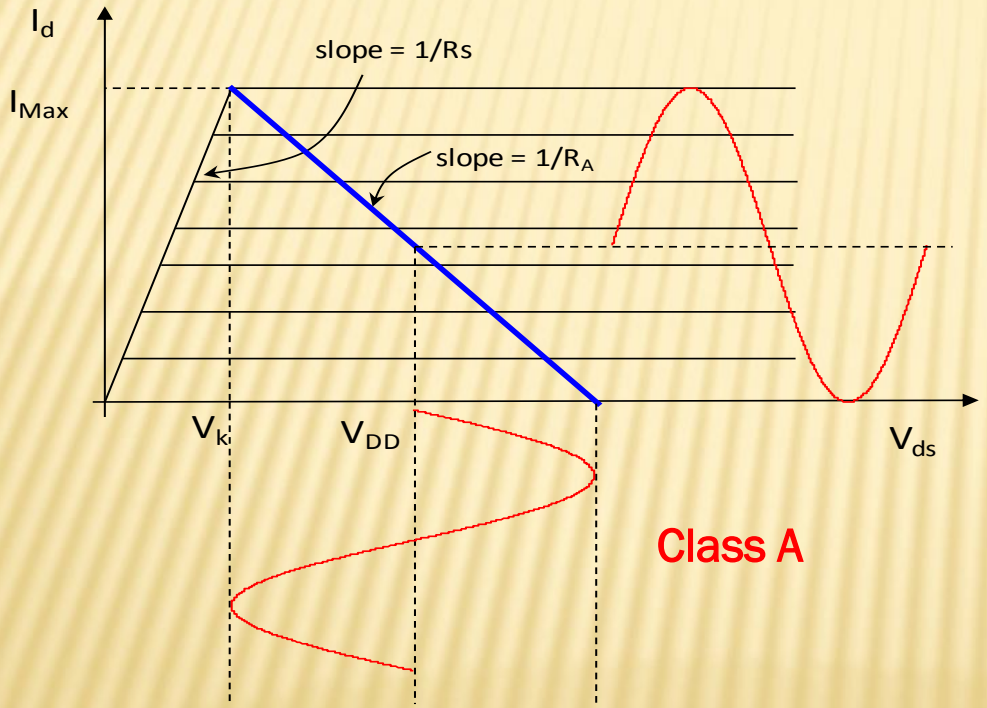
Maximum output power (and efficiency)

$\varphi=0$, i.e. purely resistive load presented to the intrinsic VCCS.

- ***Complex load → elliptic load curve***

CLASS A REFERENCE PARAMETERS

- For Class A the optimum resistive loads R_A, together with main PA features (output power at fundamental frequency $P_{RF,A}$, DC power $P_{DC,A}$, drain efficiency η_A) can be easily inferred.



Class A

$$I_P = \frac{I_{Max}}{2} \qquad V_P = V_{DD} - V_k$$

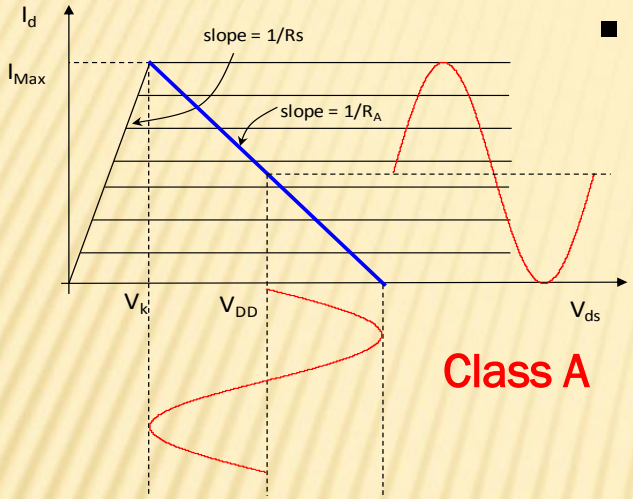
$$R_A = 2 \cdot \frac{V_{DD} - V_k}{I_{Max}}$$

$$P_{RF,A} = \frac{1}{2} \cdot (V_{DD} - V_k) \cdot \frac{I_{Max}}{2}$$

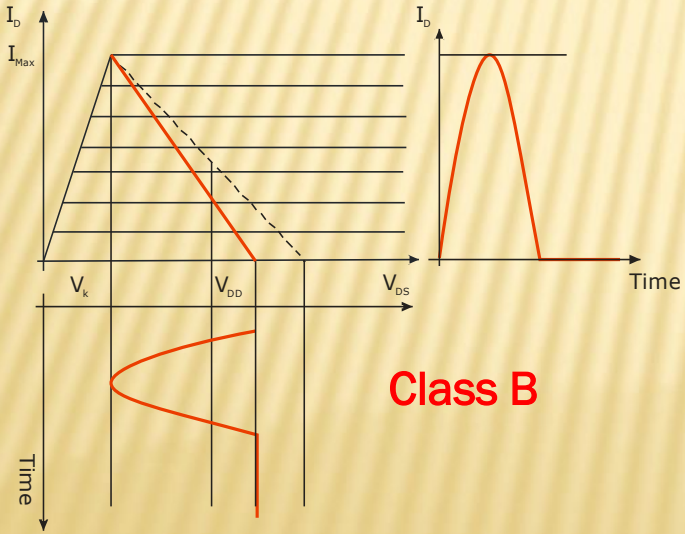
$$P_{DC,A} = V_{DD} \cdot \frac{I_{Max}}{2}$$

$$\eta_{d,A} = \frac{P_{RF,A}}{P_{DC,A}} = \frac{1}{2} \cdot \left(1 - \frac{V_k}{V_{DD}}\right)$$

RESISTIVE LOAD FEATURES



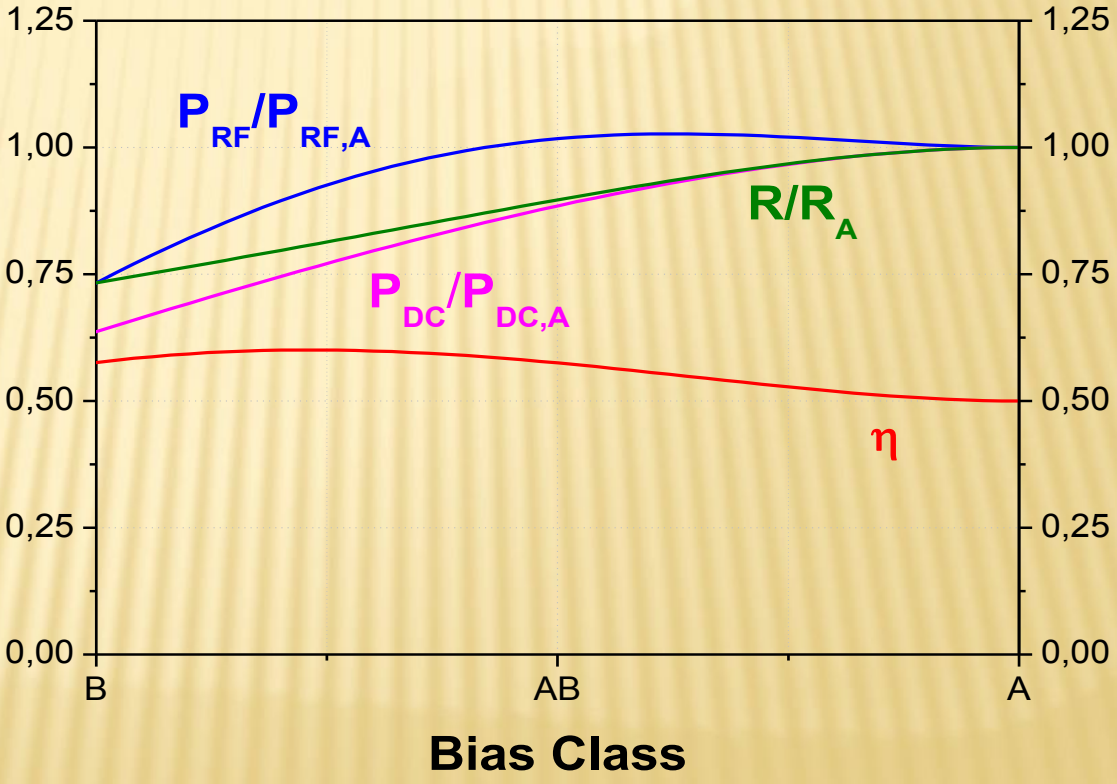
Class A



Class B

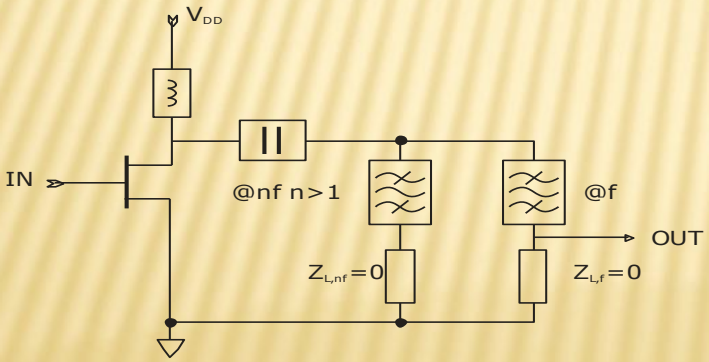
- Changing the bias point while assuming a resistive load

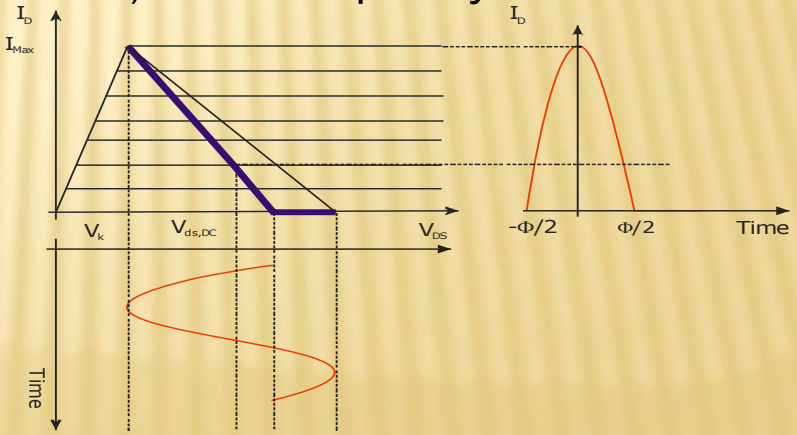
$$V_{ds}(t) = -R \cdot I_{ds}(t)$$



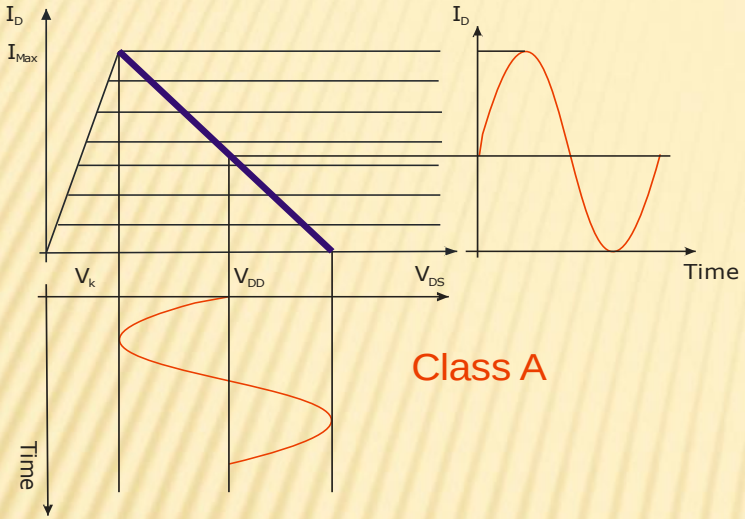
TUNED LOAD

- The output power and efficiency performances can be greatly improved by changing the bias point and making use of harmonic tuning strategies.
- To this goal, a first step resides in the use of the Tuned-Load operating mode of a power stage.
  - The device output is *short-circuited at all harmonic frequencies*
    ➔ purely sinusoidal drain (output) voltage results
  - At fundamental frequency, *current and voltage components must be in-phase* to obtain the maximum active power
    ➔ the load (at the device intrinsic terminals) must be purely resistive.

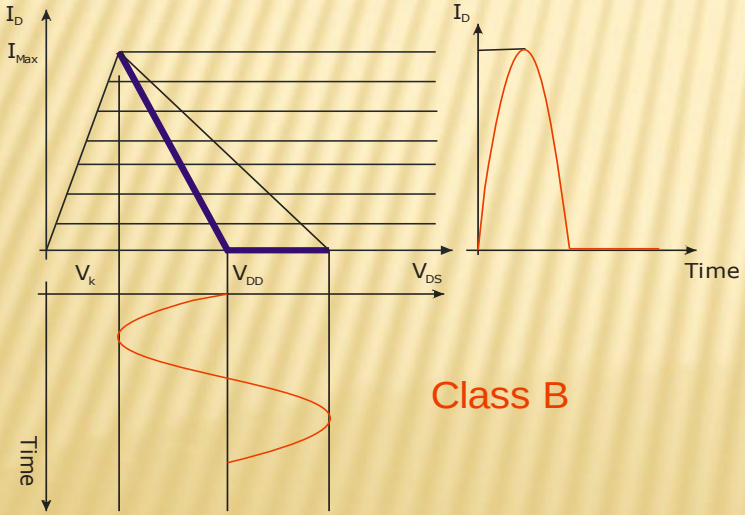




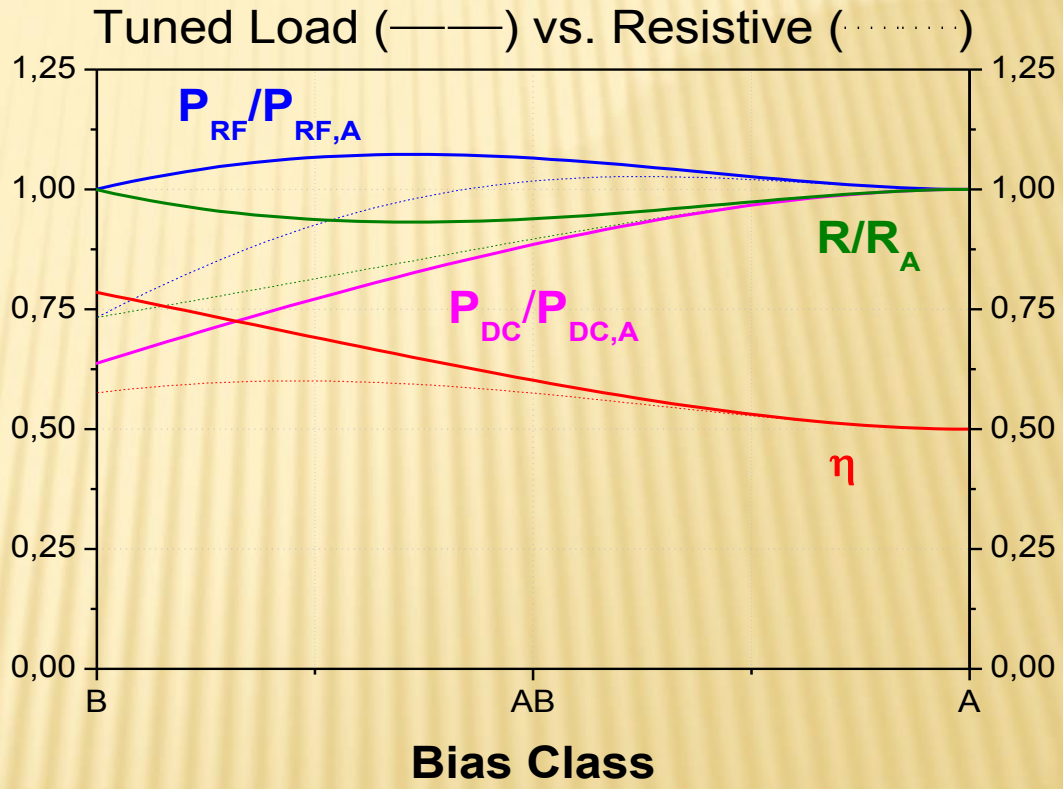
TUNED LOAD FEATURES



Class A



Class B



GAIN EVALUATION

- Assuming a Class A bias condition and maximum swing

$$P_{out,A} = \frac{1}{2}\cdot\frac{I_{Max}}{2}\cdot\left(V_{DD} - V_k\right) = \frac{I_{Max}}{4}\cdot\left(V_{DD} - V_k\right)$$

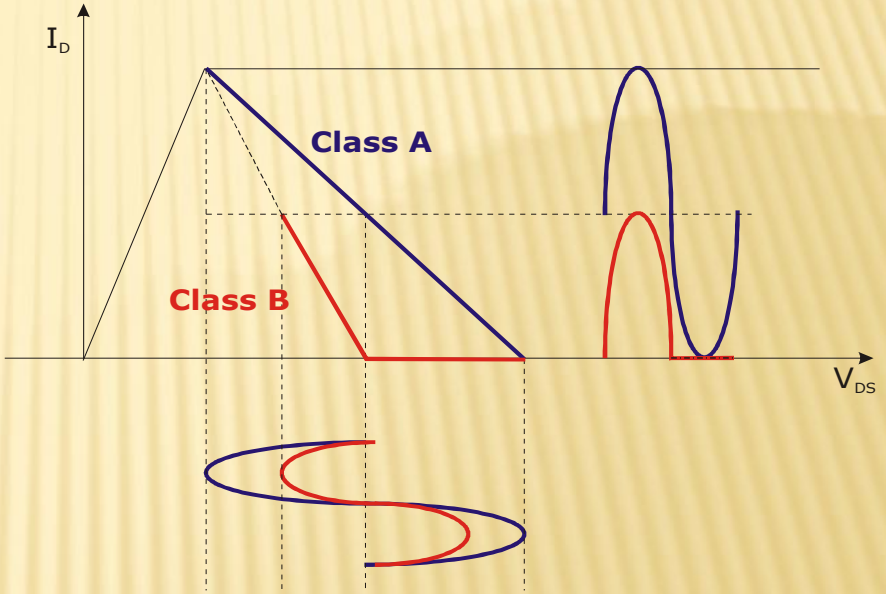
- For a Class B bias condition and the same input power level

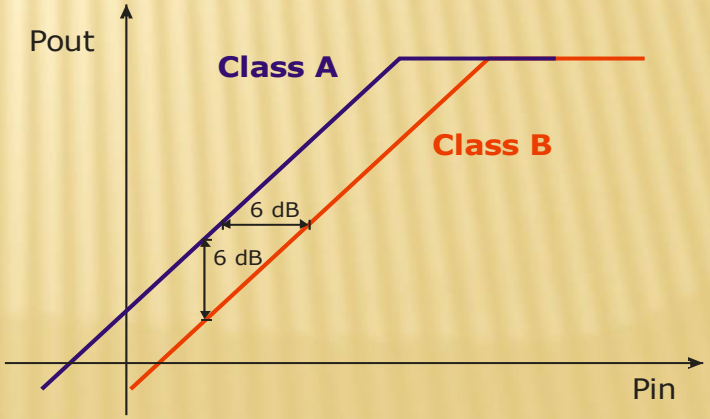
$$P_{out,B} = \frac{1}{2}\cdot\frac{I_{Max}}{4}\cdot\frac{\left(V_{DD} - V_k\right)}{2} = \frac{1}{4}\cdot P_{out,A}$$

- Thus for the gain it follows

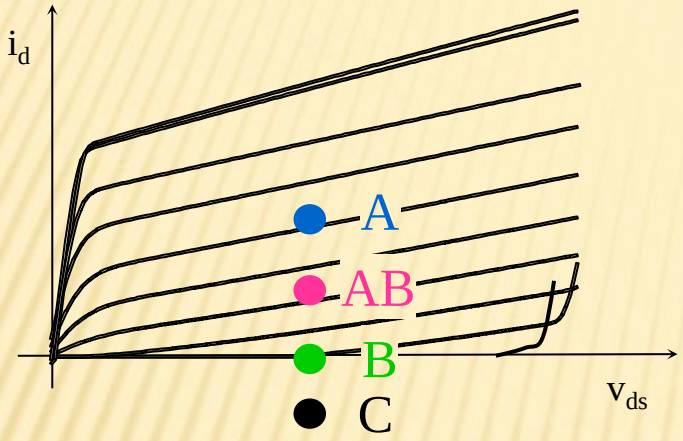
$$G_A = \frac{P_{out,A}}{P_{in}} = \frac{4\cdot P_{out,B}}{P_{in}} = 4\cdot G_B$$

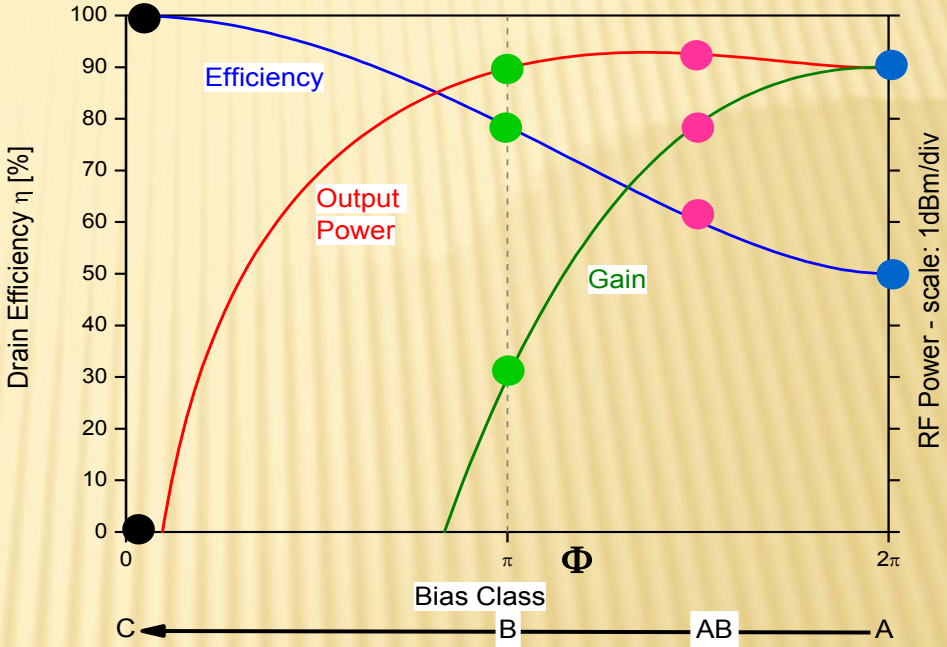
$$G_A\big|_{[dB]} = 10\cdot\log_{10} 4 + G_B\big|_{[dB]} = 6dB + G_B\big|_{[dB]}$$





TUNED LOAD DESIGN

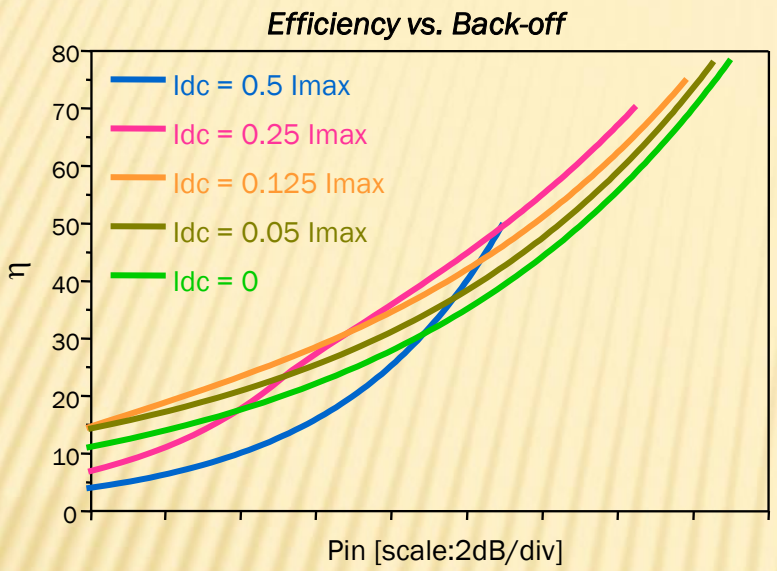


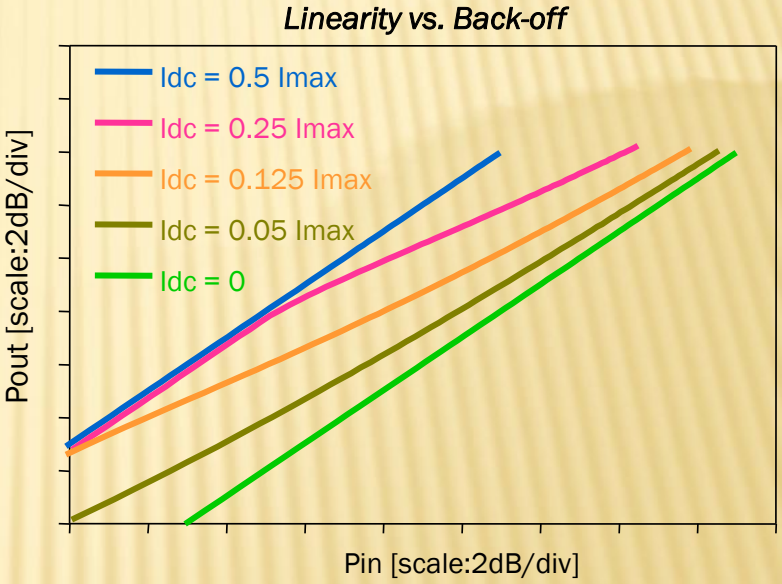


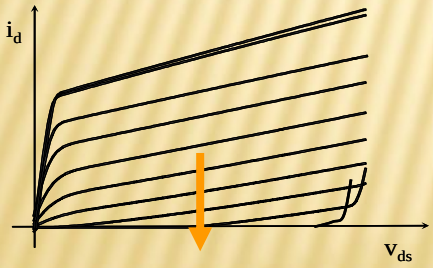
Design guidelines

- The optimum resistive load exhibits a poor dependence on Φ.
- Moving from Class-C towards Class-A increases the power dissipation on the active device and consequently decreases the efficiency.
- The input network must be designed in order to fulfil conjugate matching condition.
- The output network must be designed in order to synthesise a purely resistive load at the current source.

PA DESIGN TRADE-OFF





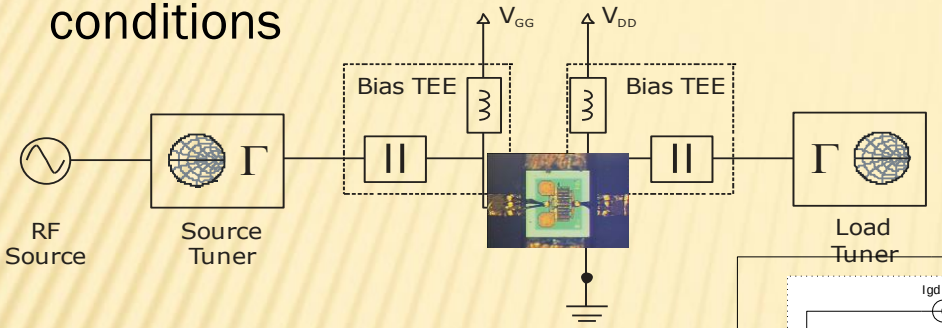


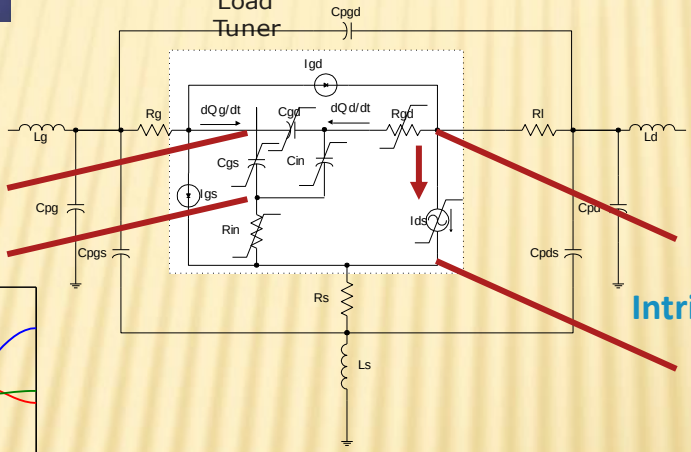
Decreasing quiescent bias point

- Highest back-off becomes mandatory to resurrect linear device behaviour (except for ideal Class B bias condition)
- Back-off operating condition rapidly decrease the efficiency

TUNED LOAD DESIGN: EXAMPLE

- Identification of external loading impedances to fulfill at the intrinsic the TL conditions

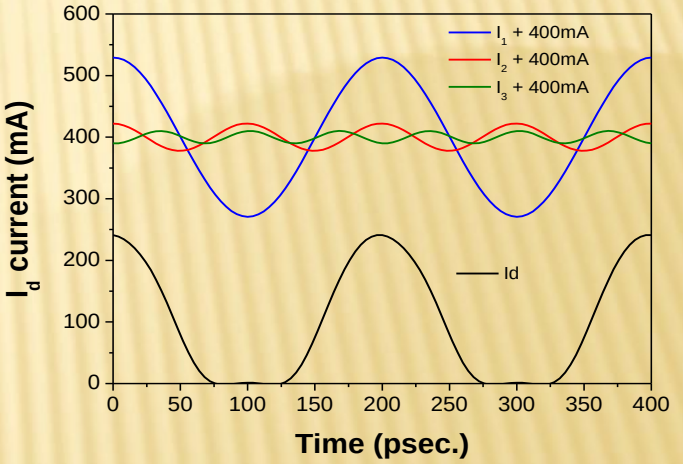


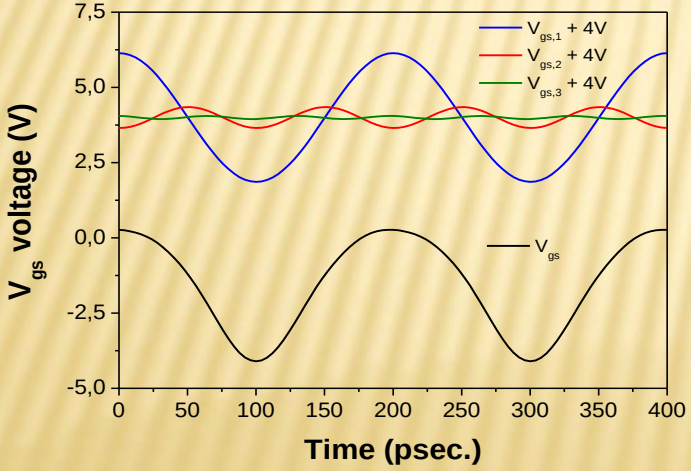


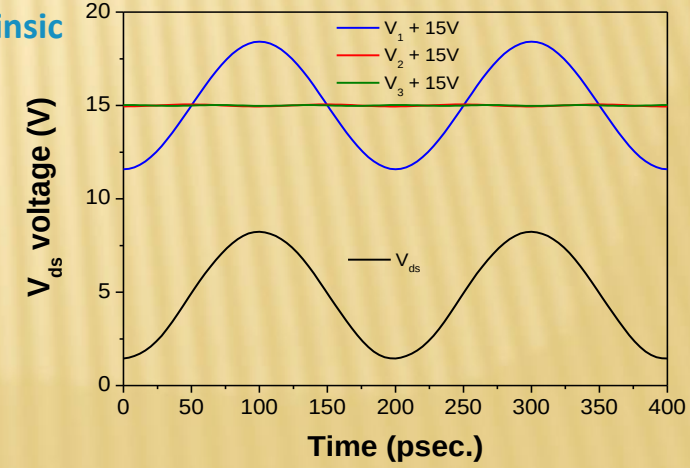
Input driving signal

Intrinsic

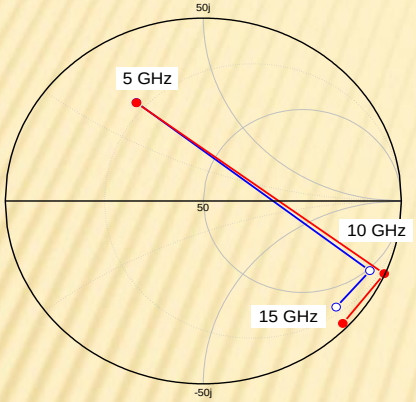
1dB compression point

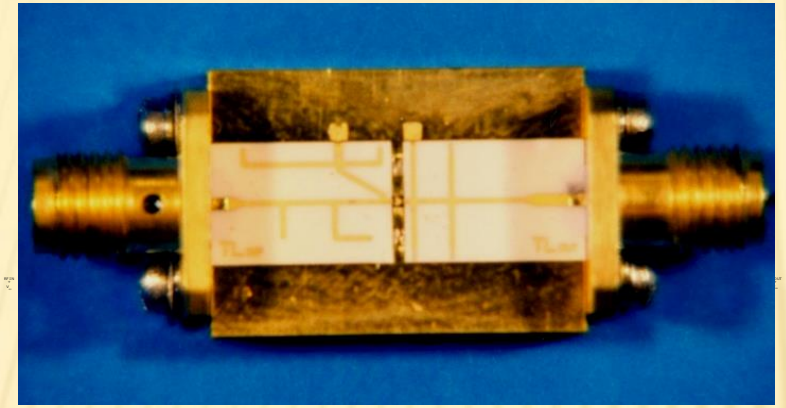


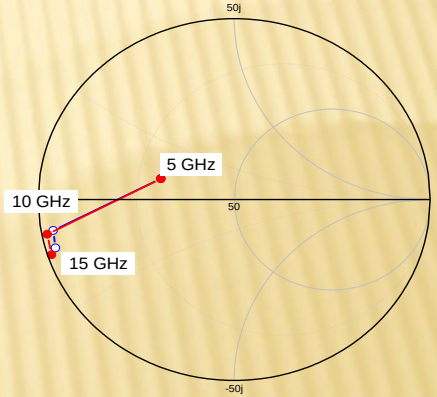


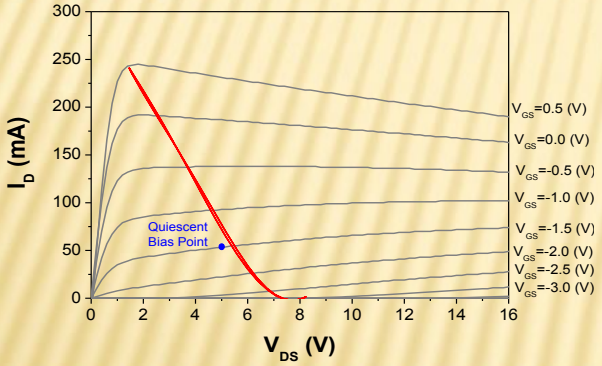


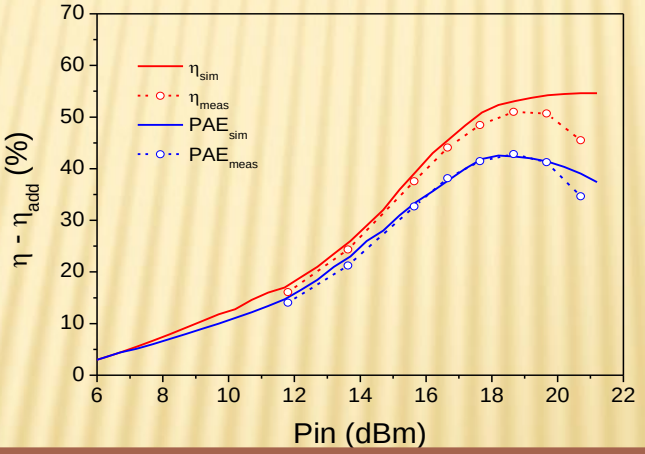
TUNED LOAD DESIGN: EXAMPLE

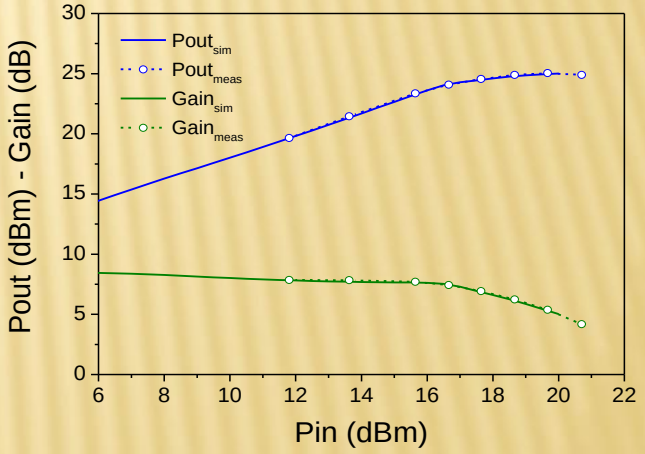








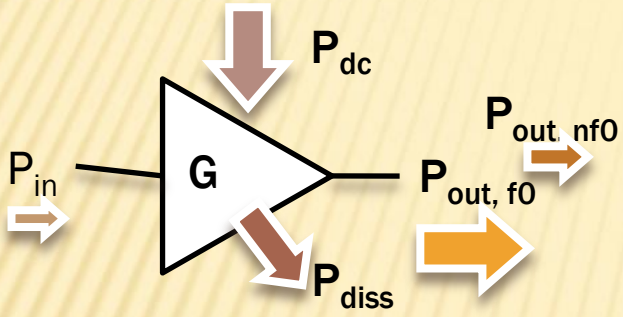




	Z_{int} (Ω)	Pout (dBm)	η (%)	PAE (%)
Simplified approach	26	23.7	48.3	/
Simulation	26.5+j0.1	24.3	50.6	42.6
Measurements	/	24.8	49.9	42.0

INCREASING EFFICIENCY

- The efficiency of a power amplifier can be described in terms of energy balance:



$$P_{dc} = P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}$$

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf}}$$

- Two conditions have to be ***simultaneously*** fulfilled to achieve maximum ideal efficiency (η =1):

$$P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t) \cdot i_D(t)\, dt = 0$$

- *No overlap between voltage and current*

$$\sum_{n=2}^{\infty} P_{out,nf} = \frac{1}{2}\sum_{n=2}^{\infty} V_n \cdot I_n \cdot \cos(\psi_n) = 0$$

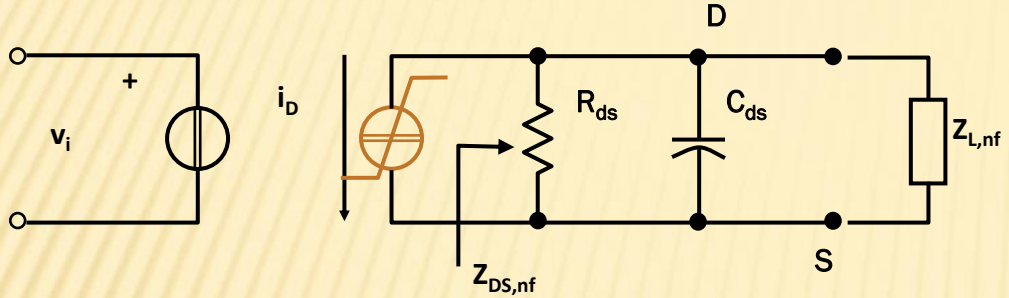
- *No power delivered at harmonics*

$$V_n \cdot I_n = 0 \quad \forall \quad n \geq 2$$

$$\cos(\psi_n) = 0 \Rightarrow \psi_n = \frac{\pi}{2} \quad \forall \; n \geq 2$$

- Current mode PAs (e.g. Class F)
- Switched mode PAs (e.g. Class E)

HARMONIC TUNING: THEORY



- The active device is represented as a nonlinear current source

- ***Current***:
  imposed by the active device and by input nonlinearities

$$i_D(t) = I_0 + \sum_{n=1}^{\infty} I_n \cos(n \cdot \omega t)$$

- ***Voltage***:
  related to the output impedance
  (only the ***first 3*** harmonics are considered)

$$v_{DS}(t) = V_{DD} - \sum_{n=1}^{M} I_n \cdot \left|Z_{DS,nf}\right| \cdot \cos\left(n \cdot \omega t + \angle Z_{DS,nf}\right)$$

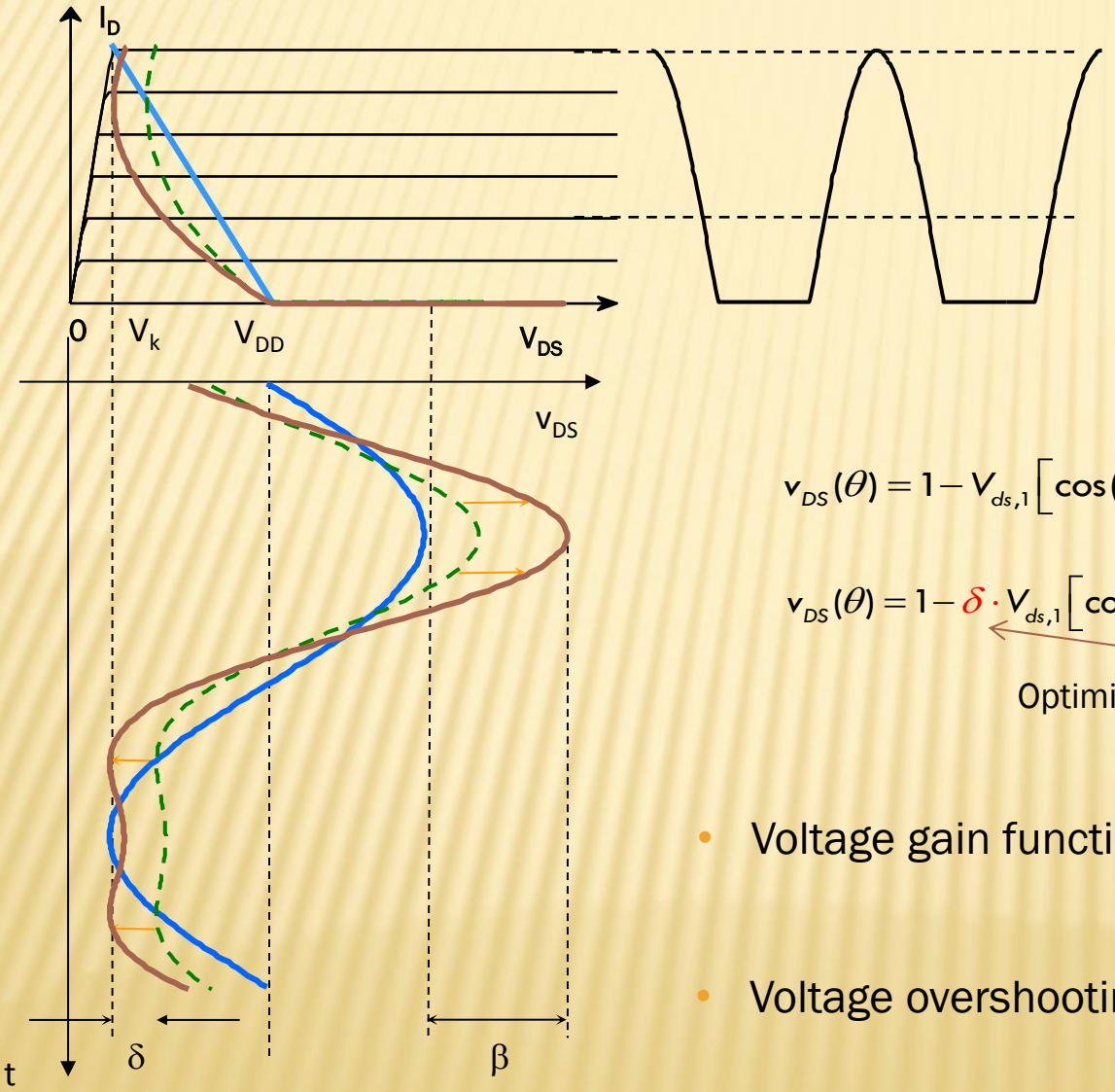
- The high efficiency condition is achieved through an appropriate shaping of the output voltage waveform, i.e. through the choice of harmonic impedances:

Max η ⇒ ***Optimization of $Z_{DS,nf}$***

$$P_{out,f} = \frac{1}{2} I_1^2 \cdot \left|Z_{DS,f}\right| \cdot \cos\left(\angle Z_{DS,f}\right) \qquad V_k \le v_{DS}(t) \le V_{BD}$$

Also the ***input*** harmonics terminations and the ***bias point*** have a strategic role!

HARMONIC TUNING: ADDING A 2ND HARMONIC



$$v_{DS}(t) = V_{DD} - V_1 \cdot \left[\cos(\omega t)\right]$$

Insertion of a 2nd harmonic component

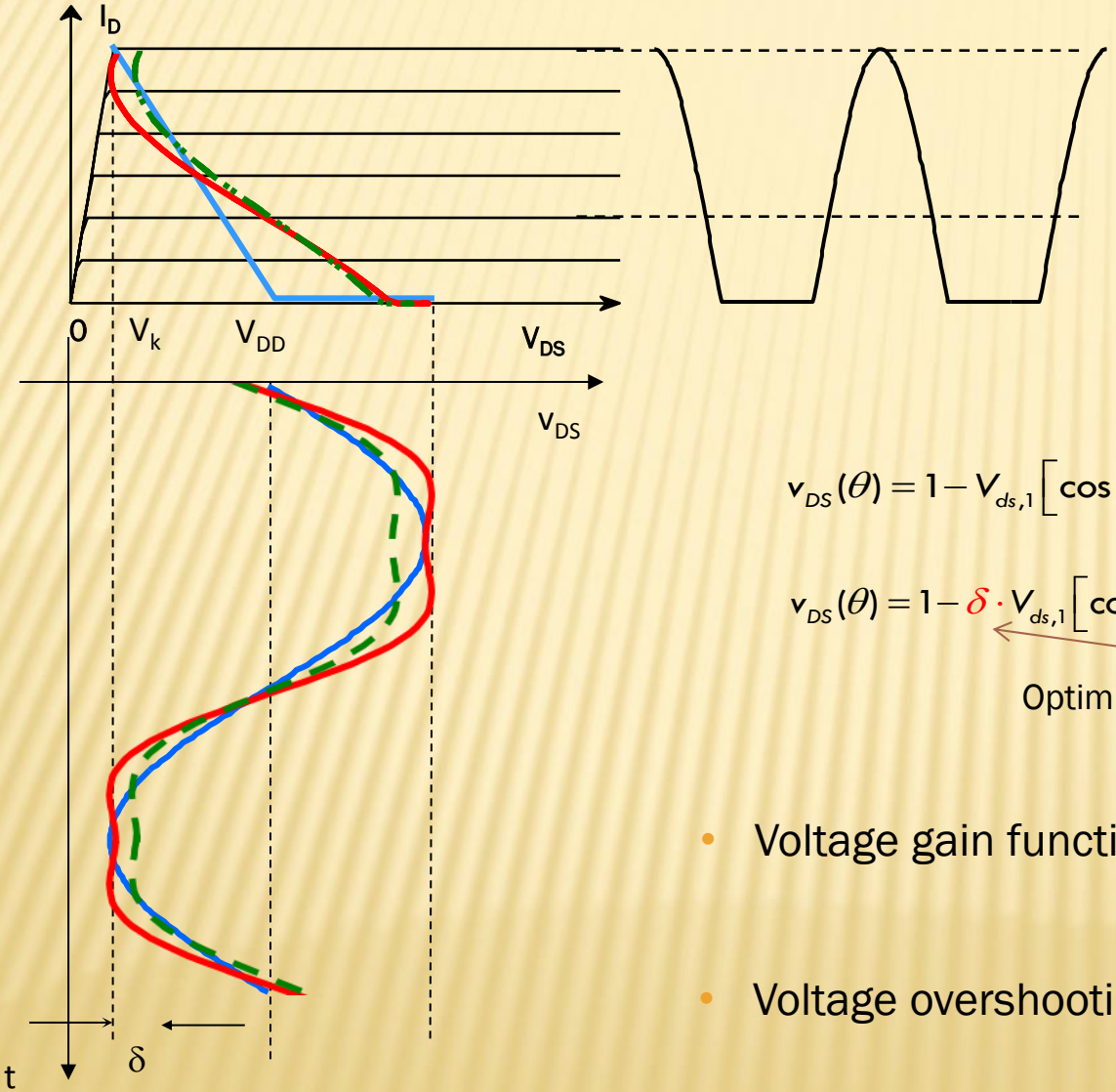
$$v_{DS}(\theta) = 1 - V_{ds,1}\left[\cos(\theta+\phi) + \cos\left[2(\theta+\phi)\right]\right]$$

$$v_{DS}(\theta) = 1 - \delta \cdot V_{ds,1}\left[\cos(\theta+\phi) + k_2 \cos\left[2(\theta+\phi)\right]\right] \qquad k_2 = \frac{V_2}{V_1}$$

Optimization of *1st* and *2nd* harmonic components

- Voltage gain function $\delta(k_2) \equiv \dfrac{V_1}{V_{1,TL}} = 1.41$
- Voltage overshooting function $b(k_2) = \dfrac{V_{DS,max} - V_{DD}}{V_{DD}} = 1.91$

HARMONIC TUNING: ADDING A 3RD HARMONIC



$$v_{DS}(t) = V_{DD} - V_1 \cdot \left[\cos(\omega t)\right]$$

Insertion of a *3rd* harmonic component

$$v_{DS}(\theta) = 1 - V_{ds,1}\left[\cos(\theta+\phi) + \cos\left[3(\theta+\phi)\right]\right]$$

$$v_{DS}(\theta) = 1 - \delta \cdot V_{ds,1}\left[\cos(\theta+\phi) + k_3 \cos\left[3(\theta+\phi)\right]\right] \qquad k_3 = \frac{V_3}{V_1}$$

Optimization of *1st* and *3rd* harmonic components

- Voltage gain function $\delta(k_3) \equiv \dfrac{V_1}{V_{1,TL}} = 1.15$
- Voltage overshooting function $b(k_3) = \dfrac{V_{DS,max} - V_{DD}}{V_{DD}} = 1$

HARMONIC TUNING: DESIGN GUIDELINES

	k2	k3	δ	β
Tuned Load	0	0	1	1
Class F (3rd HT)	0	-0.17	*1.15*	1
2nd HT	-0.35	0	*1.41*	1.91
2nd & 3rd HT	-0.55	0.17	*1.62*	2.81

- **Immediate evaluation of PA performance:**

$$G_{HT} = G_{TL} \cdot \delta(k_2, k_3) \qquad P_{out,f,HT} = P_{out,f,TL} \cdot \delta(k_2, k_3)$$

$$\eta_{HT} = \eta_{TL} \cdot \delta(k_2, k_3) \qquad \eta_{add,HT} = \eta_{add,TL} + \left[\delta(k_2, k_3) - 1\right] \cdot \eta_{d,TL}$$

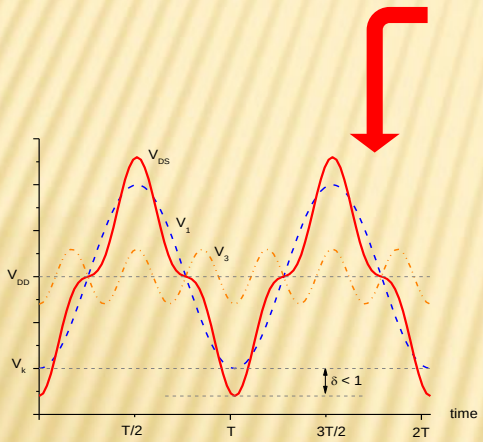
- **Design guidelines** ⇒

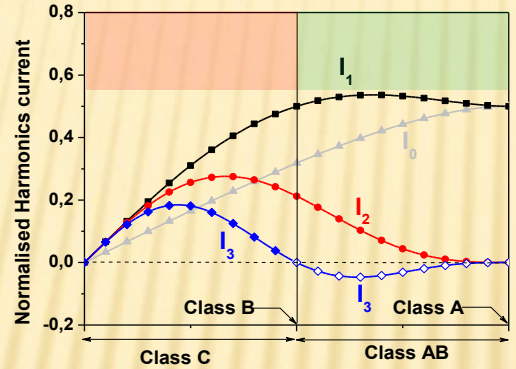
$$R_{f,HT} = \delta(k_2, k_3) \cdot R_{TL}$$

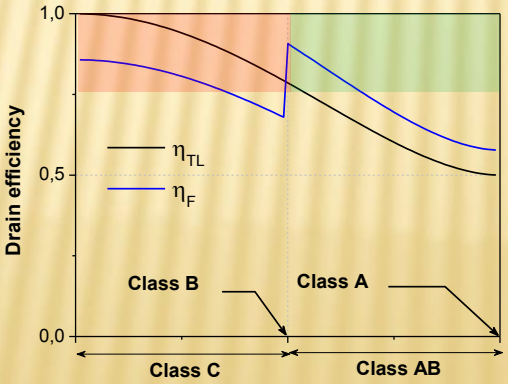
$$R_{nf,HT} = \delta(k_2, k_3) \cdot k_n \frac{V_{DD}}{I_n} \qquad n = 2,3$$

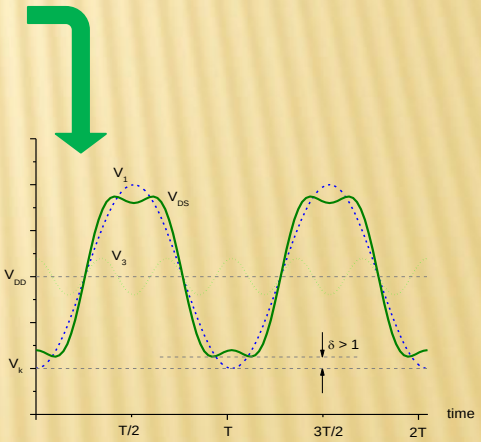
CLASS F IDEAL: REMARKS !!!

- A 100% drain efficiency depends on perfect terminations (***0 - even***, ***∞ - odd*** harmonics)
- In actual cases, only few harmonics can be practically controlled (***0 - f >3fo***)
- Nothing is said about the voltage harmonic generation mechanism
- The “phase” of the harmonics is not considered
- The role of device output resistance R_{DS} is not evidenced

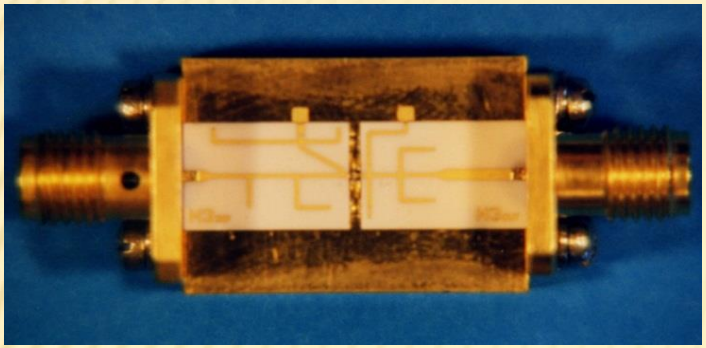


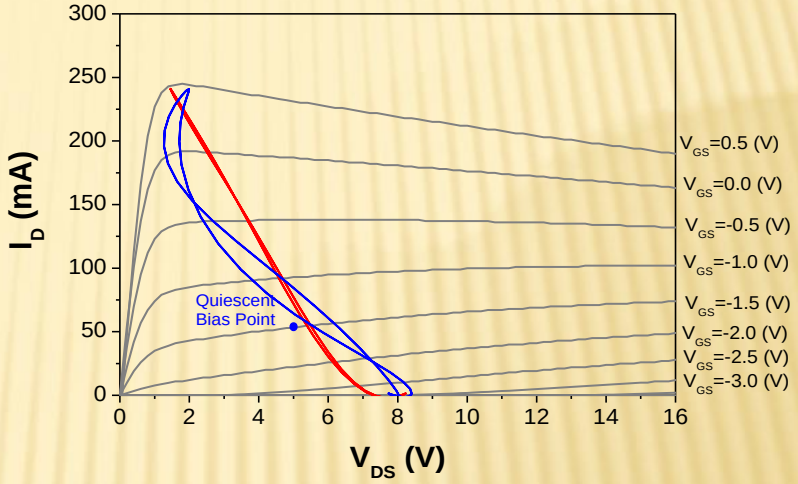


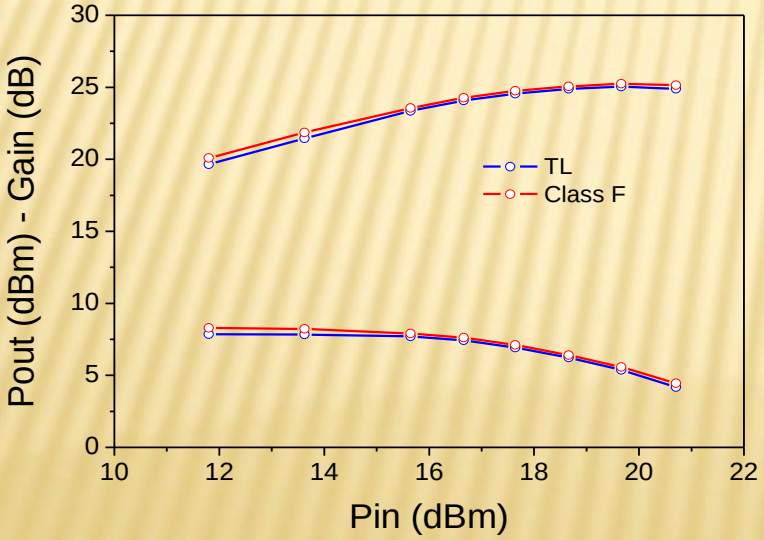


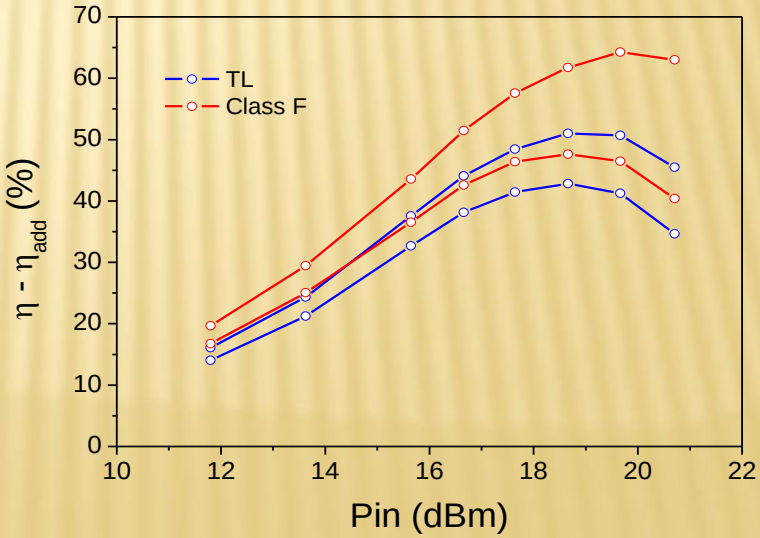


CLASS F DESIGN EXAMPLE



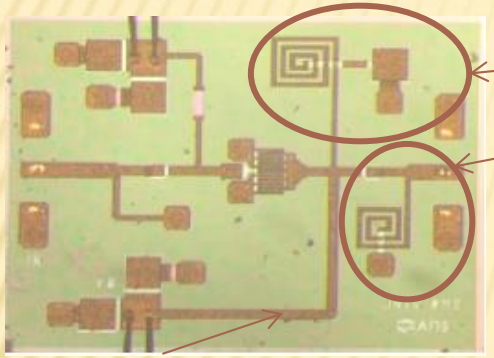




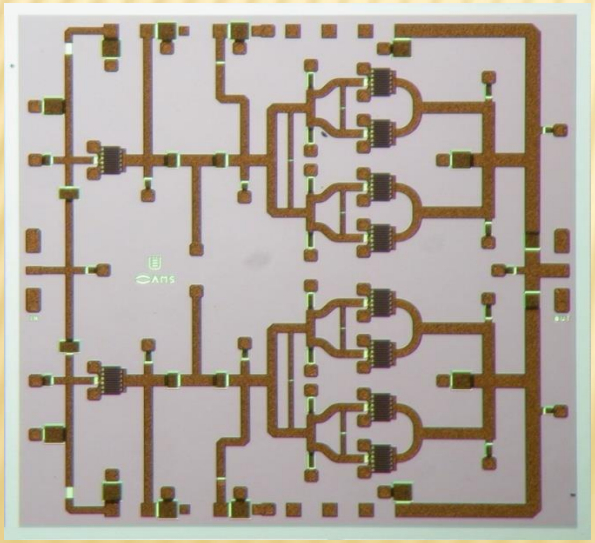


HARMONIC TUNING: EXAMPLES

GaAs X-band Class F amplifiers

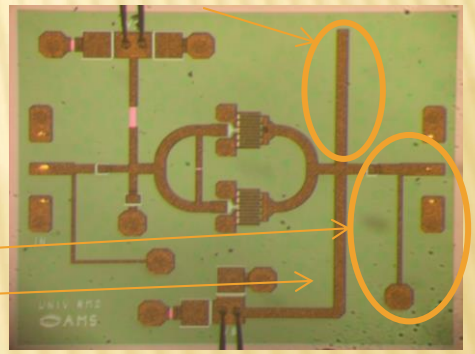


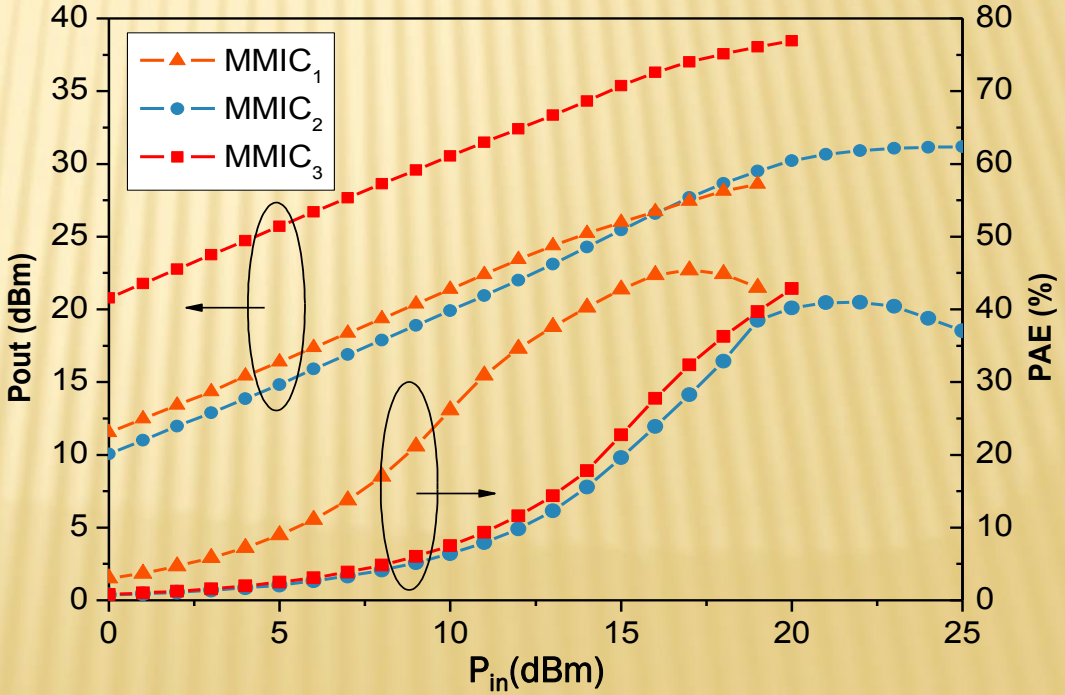
MMIC 1
1.5 x 1.9 mm²
P_{out} = 0.5W
PAE = 44%



MMIC 3
4.7 x 4.7 mm²
P_{out} = 7W
PAE = 40%

MMIC 2
1.8 x 2.3 mm²
P_{out} = 1W
PAE = 40%





HARMONIC TUNING: REMARKS!

- The obtained results have to be carefully managed!
  - The potential improvements are true ***if and only if*** the drain current harmonic components have proper phase relationships to allow $R_{nf} > 0$ (physical)
  - The correct phase relation mostly depends upon ***bias point*** of the device

Example: 2nd HT PA

To design a 2nd HT PA, the following intrinsic impedances have to be synthesised

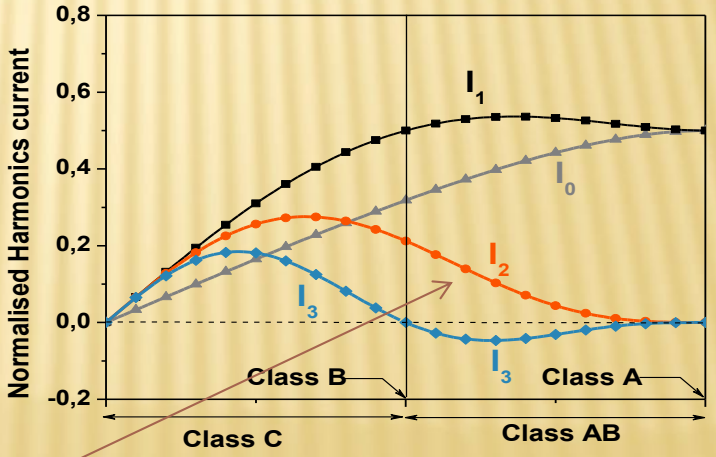
$$R_f = 1.41 \cdot \frac{V_{DD}}{I_1} \qquad R_{2f} = 1.41 \cdot (-0.35) \cdot \frac{V_{DD}}{I_2} \qquad R_{3f} = 0$$

Therefore two conditions have to be fulfilled

$R_f > 0 \Rightarrow I_1 > 0$

$R_{2f} > 0 \Rightarrow I_2 < 0$

I_1 and I_2 must be out of phase !!!



Theoretically, is not possible to design a 2nd HT PA in "normal" conditions

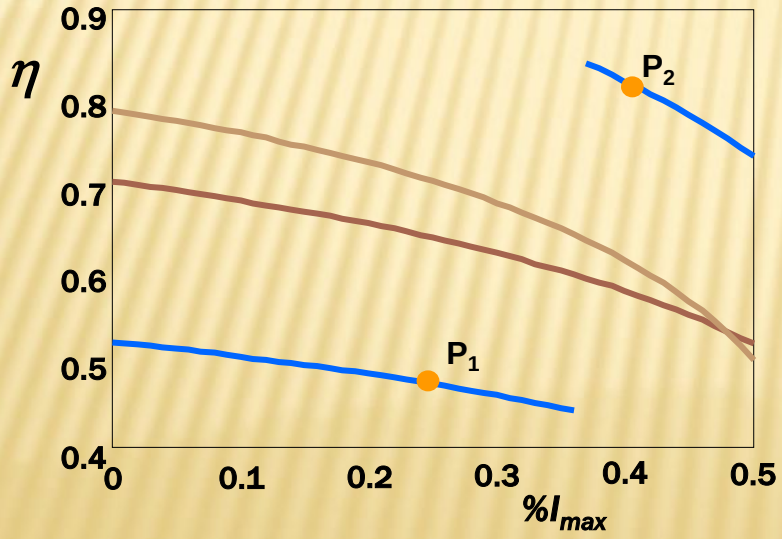
HARMONIC TUNING: REMARKS!

***INPUT** Harmonic Tuning*

- The input non linear effects can be used to "modify" phase relationships

$$i_D(t) = \begin{cases} I_{DD} + A_1 \cdot \cos(\omega t) + A_2 \cdot \cos(2\omega t) & if\ -\alpha/2 \le \omega t \le \alpha/2 \\ 0 & otherwise \end{cases}$$

- A_1 and A_2 related by g_m to the input voltage controlling harmonic components
  - Generated by properly loading device input non linearity (usual case)
  - By external injection (unusual !)



$A_2/A_1=0$

$R_{@f}=R_{TL}$

$R_{@nf}=0$

$A_2/A_1=-0.2$

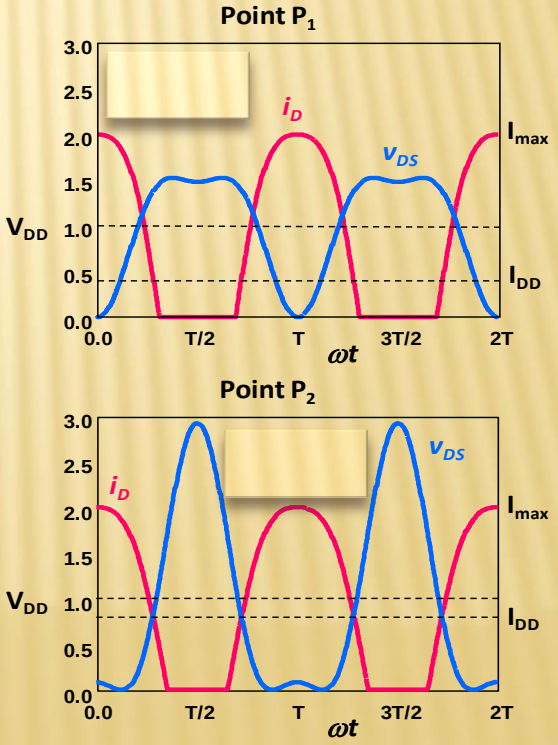
$R_{@f}=R_{TL}$

$R_{@nf}=0$

$A_2/A_1=-0.2$

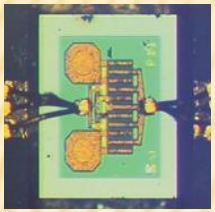
$R_{@f}=R_{2HT,f}$

$R_{@2f}=R_{2HT,2}$



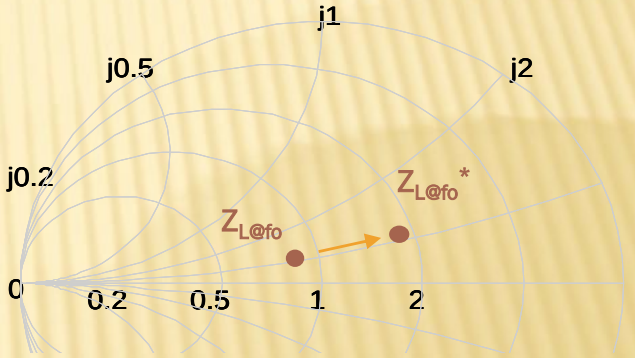
HARMONIC TUNING: DESIGN EXAMPLE

Harmonic load/source pull design example

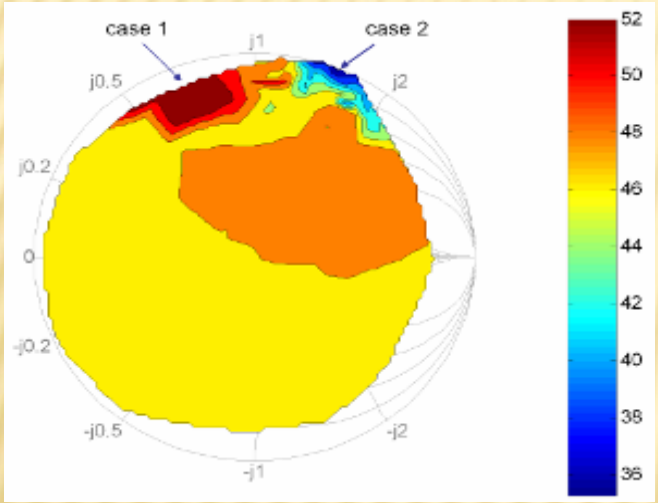


- GaAs MESFET (0.5μm x 1mm)
- Frequency: 1 GHz

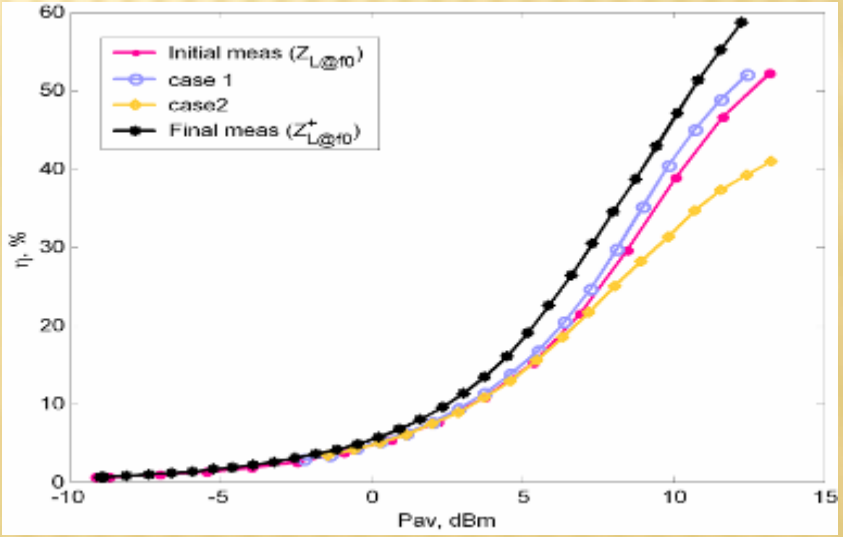
- Load Pull on Z_L @ f_0
  - Z_L @ f_0 = 40.0+6.3j Ω
  - **η@1dBcp = 46%**



- Re-Load Pull on Z_L @ f_0 (1dBcp)
  - Z_L shifts along constant susceptance from 40.0+6.3j Ω to 78.3+j23.1 Ω
  - η increases from 49% to 60%



- Source Pull on Z_S @ $2f_0$ (1dBcp)
  - Case 1 – maximum η = 49%
  - Case 2 – minimum η = 36%

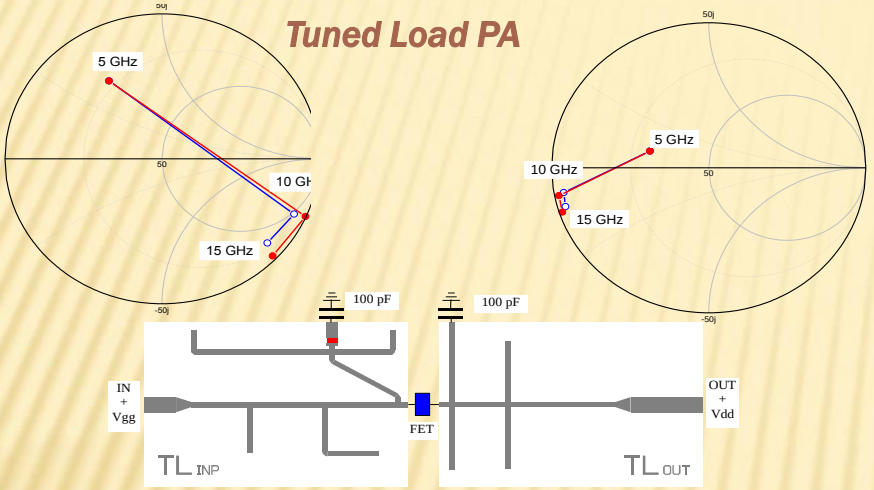


GAAS HARMONIC TUNED PAS (1/2)

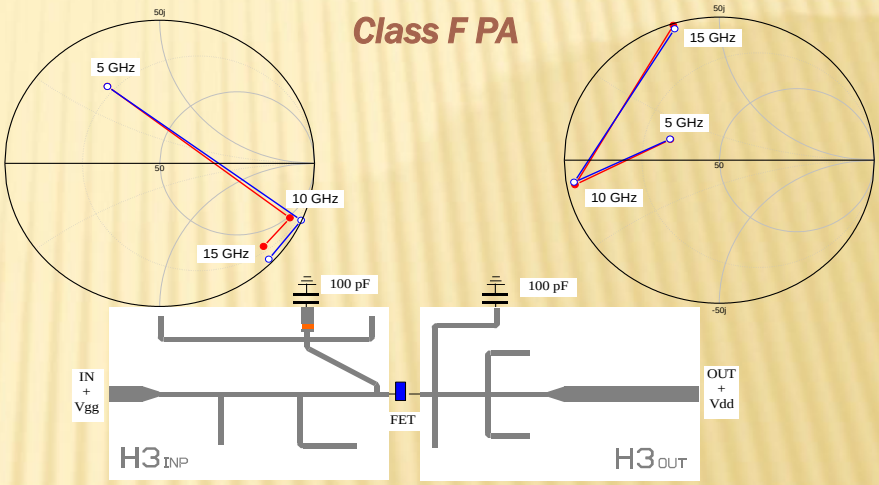
Harmonic tuned PAs design examples

- Ideal loads
- Realised loads

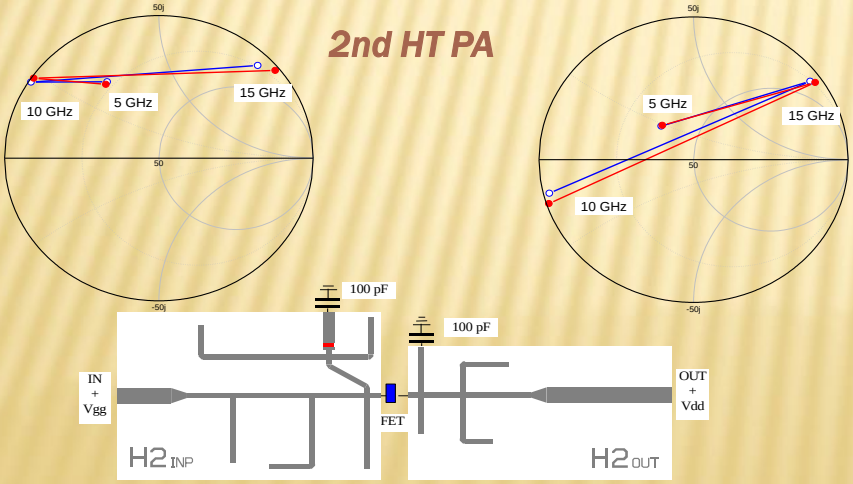
Tuned Load PA



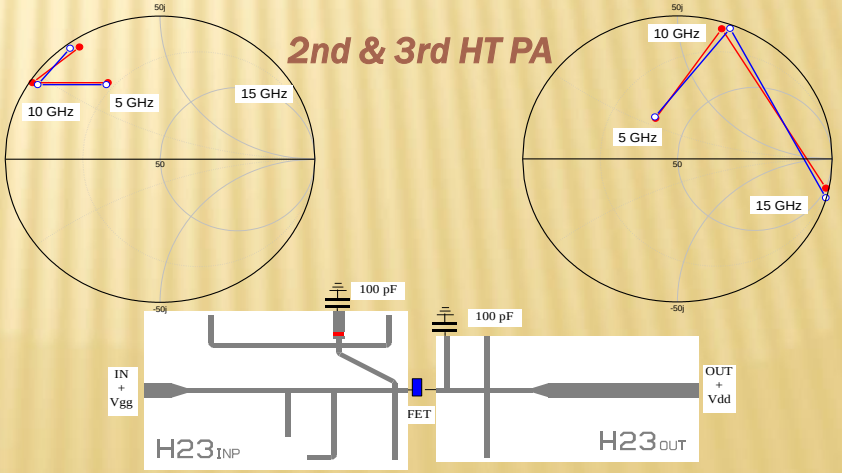
Class F PA



2nd HT PA

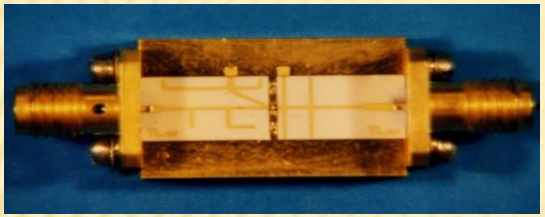


2nd & 3rd HT PA

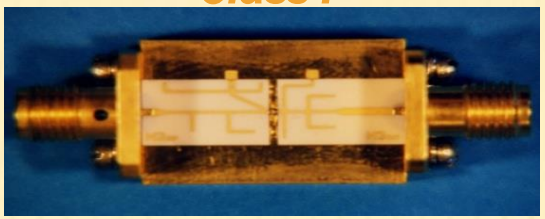


GAAS HARMONIC TUNED PAS (2/2)

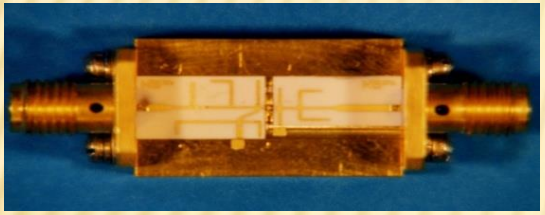
Tuned Load



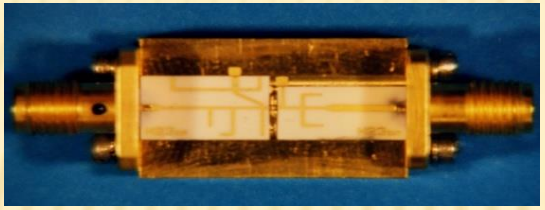
Class F

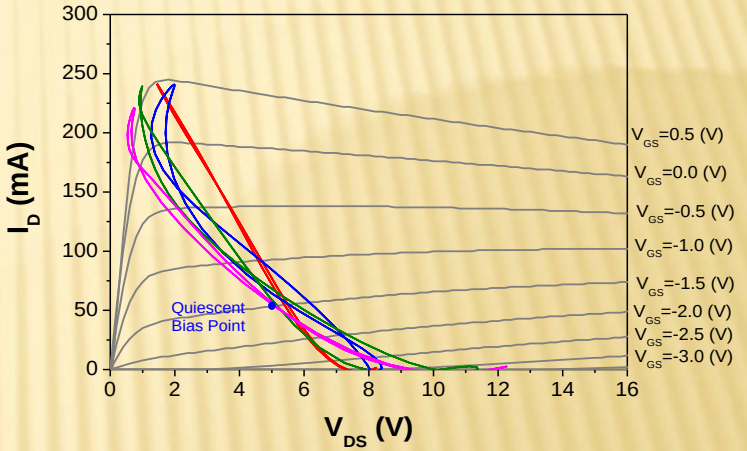


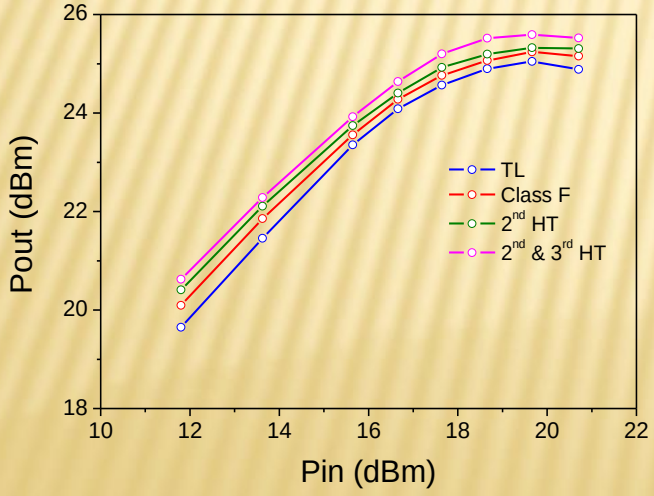
2nd HT

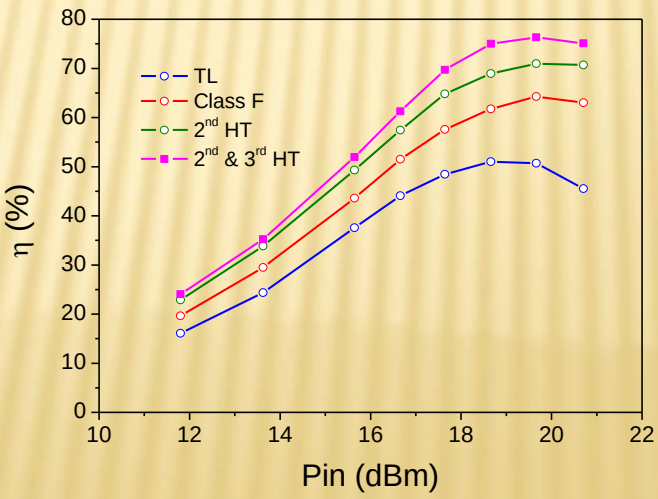


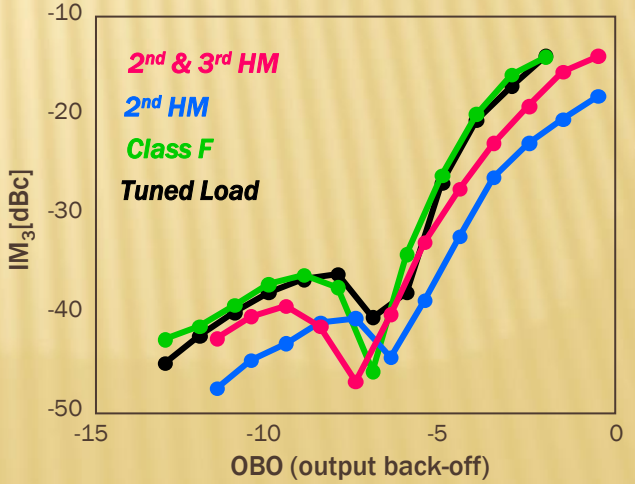
2nd – 3rd HT



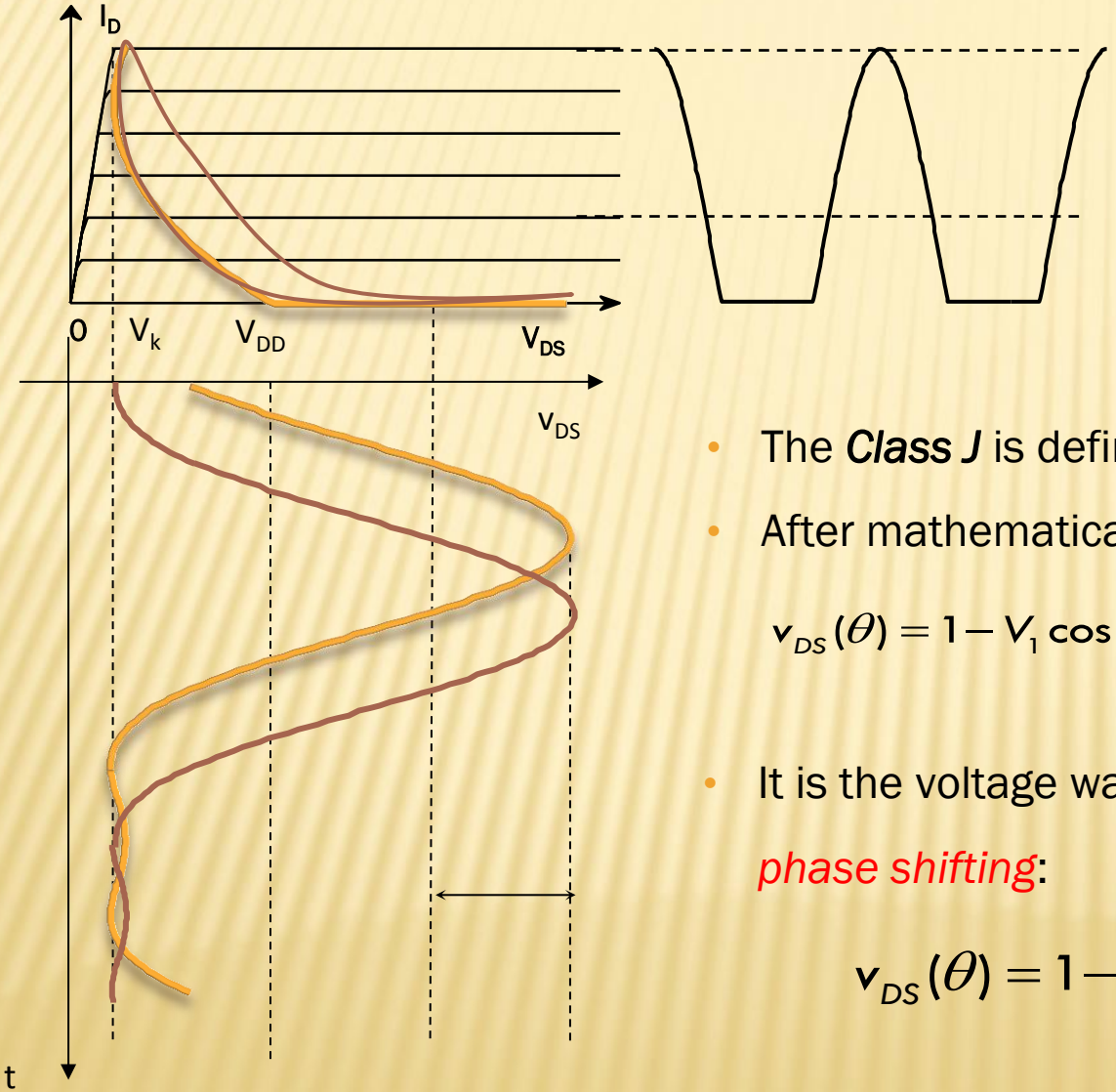








HARMONIC TUNING: THE CLASS J OPERATION



- In PAs, it is possible to define a continuous set of voltage waveforms

$$v_{DS}(\theta) = \left[1 - \alpha\cos(\theta)\right]\left[1 - \beta\sin(\theta)\right]$$

- The ***Class J*** is defined when $\alpha=\beta=1$
- After mathematical manipulation we obtain:

$$v_{DS}(\theta) = 1 - V_1\cos\left(\theta - \frac{\pi}{4}\right) - V_2\cos\left(2\theta - \frac{\pi}{2}\right)$$

- It is the voltage waveform of a ***2nd HT PA***, ***except*** *for the phase shifting*:

$$v_{DS}(\theta) = 1 - V_1\cos(\theta) - V_2\cos\left[2(\theta)\right]$$

HARMONIC TUNING: THE CLASS J OPERATION

- The phase shift in the voltage waveform implies different load conditions:

$$|V_{ds,1}| = \sqrt{2}\cdot|V_{1,TL}|, \quad \phi_1 = -\frac{\pi}{4}$$

- Complex load at f_0 ⇒ $Z_{1,J} = (1+j)R_{TL}$

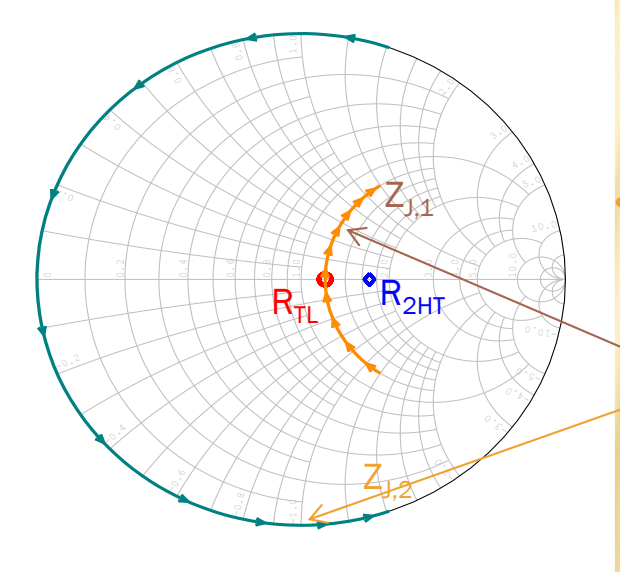
$$|V_{ds,2}| = \frac{1}{\sqrt{2}}\cdot|V_{2,TL}|, \quad \phi_2 = -\frac{\pi}{2}$$

- Reactive load at $2f_0$ ⇒ $Z_{2,J} = -j\frac{3\pi}{8}R_{TL}$

- Performances are ***unchanged*** with respect to a ***TL PA*** ⇒

$$P_{out,J} = \frac{1}{2}\mathrm{Re}\left\{Z_{1,J}I_1^{\,2}\right\} = P_{out,TL}$$

$$\eta_J = \eta_{TL}$$



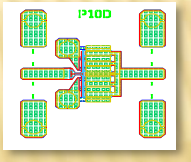
However

- Output performances are less sensitive to frequency:
  - ***wideband behaviour can be achieved***
  - Fundamental and 2nd harmonic impedances corresponding to constant output power and efficiency

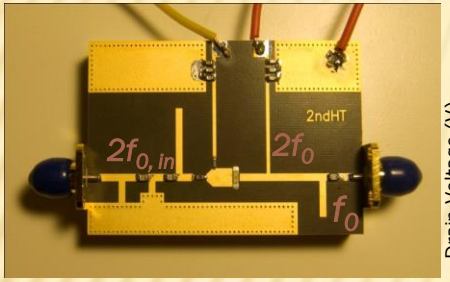
HARMONIC TUNING: DESIGN EXAMPLES

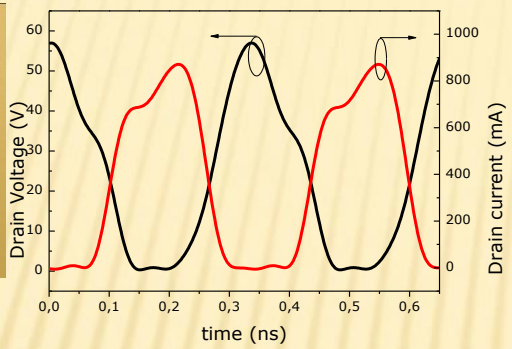
2nd Harmonic Tuned PA* vs. *Class J PA

- GaN HEMT on SiC (0.5μm x 1mm) – Selex ES
- Frequency: 3 GHz

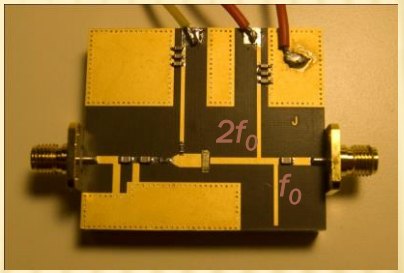


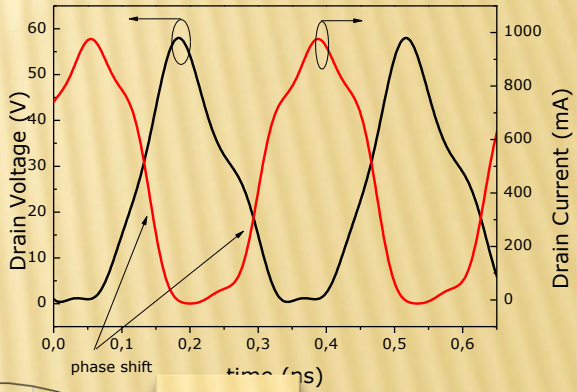
2nd HT PA

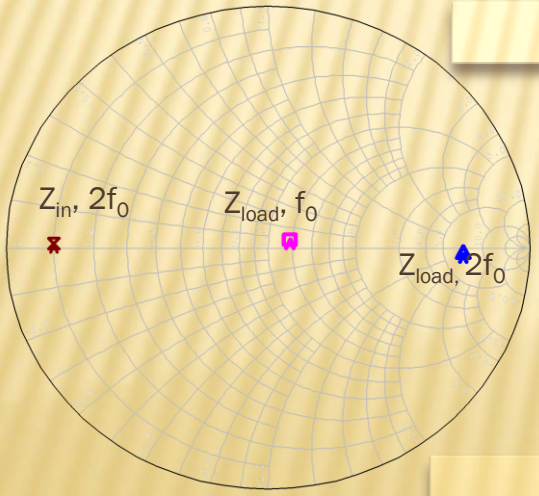


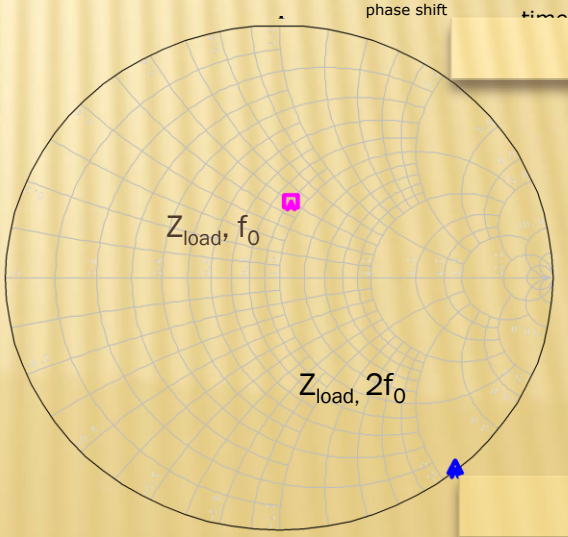


Class J PA



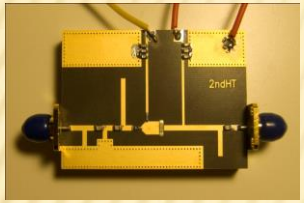


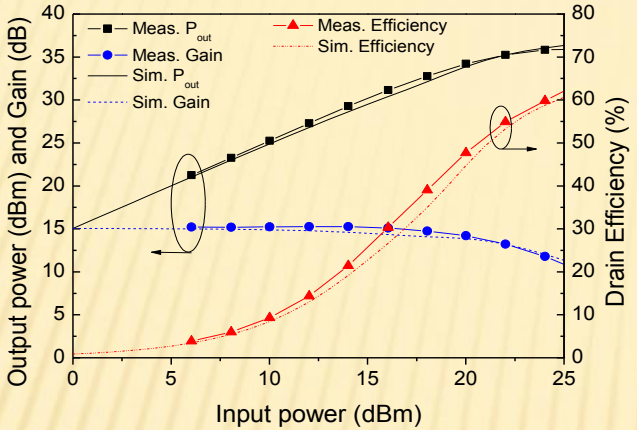


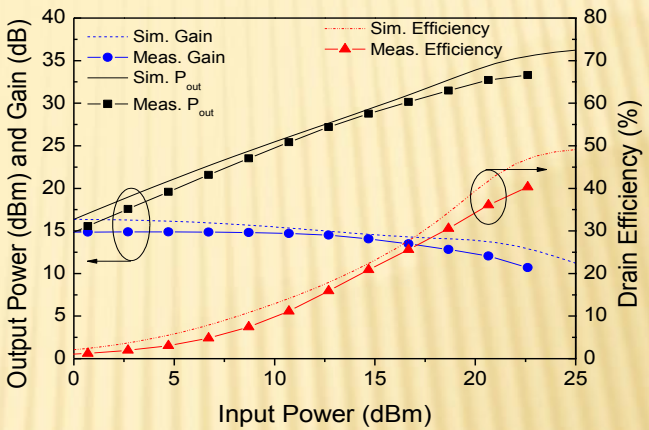


HARMONIC TUNING: DESIGN EXAMPLES

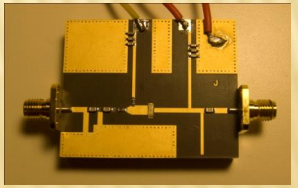
2° HT PA





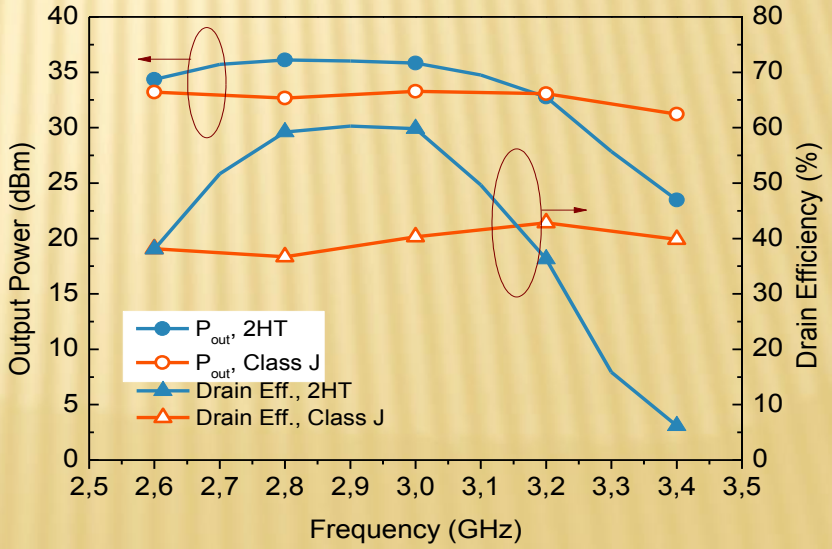


Class J PA



Performance comparison

Parameter	2ndHT PA	Class J PA
$Z_{1\ (load)}$	(59 + j4) Ohm	(45 + j30) Ohm
$Z_{2\ (load)}$	(340 - j38) Ohm	(1 - j108) Ohm
$Z_{2,in}$	(5 + j0.5) Ohm	/
Efficiency at 3 GHz	56 % (meas *57%)*	46 % (meas *39%*)
Output power at 3 GHz	*37 dBm* (meas 35 dBm)	*36 dBm* (meas 33 dBm)
Bandwidth	300 MHz	700 MHz
% Bandwidth	*10 %*	***27 %***



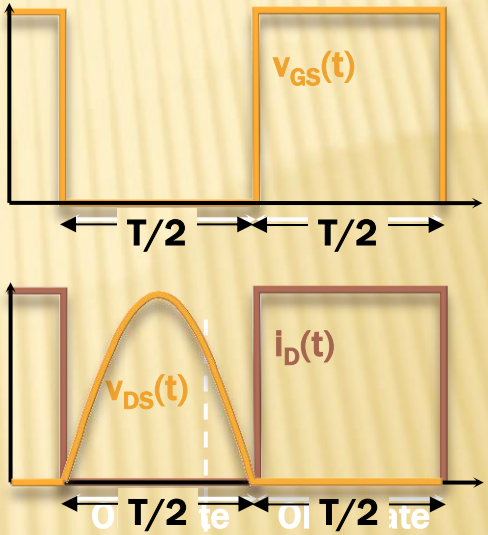
CLASS F^{-1} PA: AN IDEAL APPROACH

- Being the dual version of Class F, the Class F^{-1} requires a squared current waveform generated by a squared gate voltage
- In order to have physical realizable loads at harmonics, two conditions have to be fulfilled, as in the 2nd HT PA:

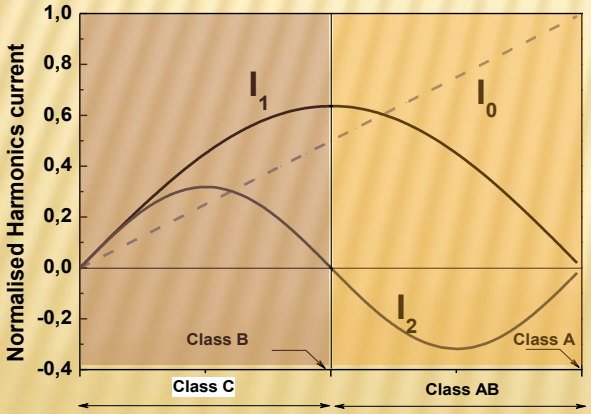
$R_f > 0 \Rightarrow I_1 > 0$

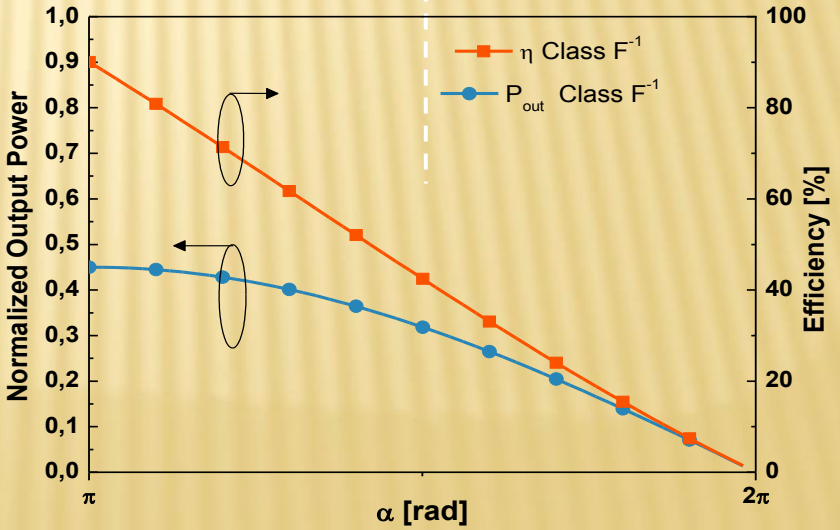
$R_{2f} > 0 \Rightarrow I_2 < 0$

I_1 and I_2 must be out of phase !!!



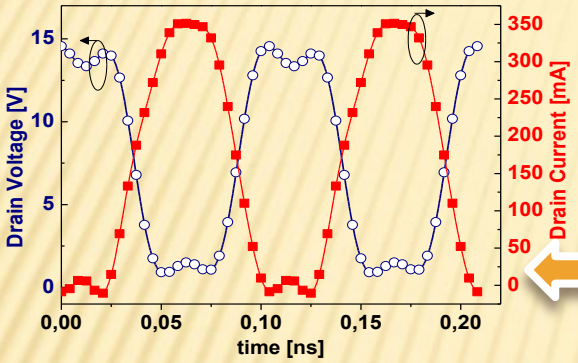
- Conditions fulfilled for $\alpha > \pi$ (***Rectangular*** current waveform)
- As approaching $\alpha = 2\pi$, performances decrease!

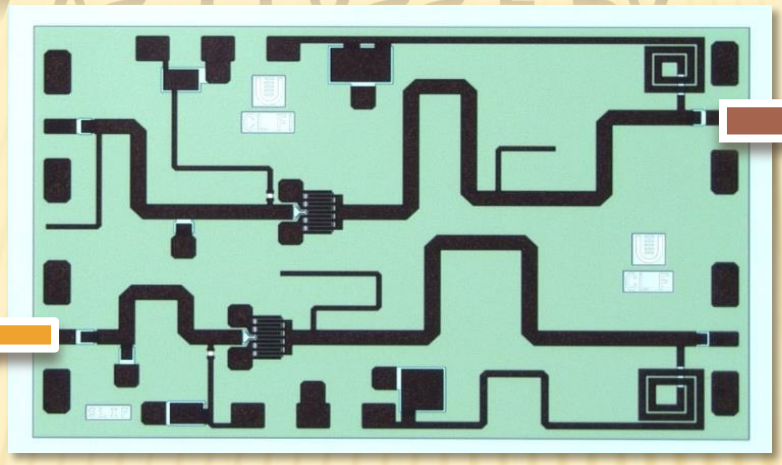




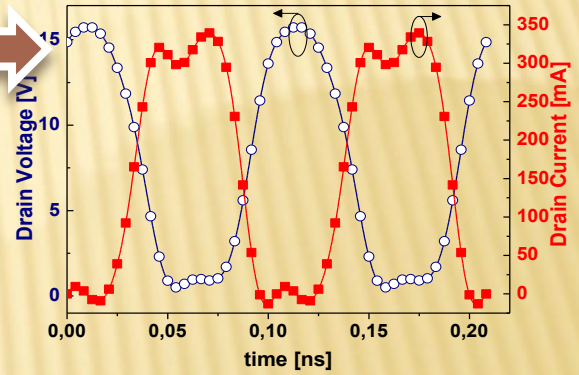
CLASS F-1 PA VS. CLASS F PA

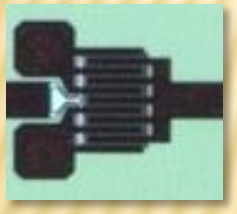
Class F drain waveforms



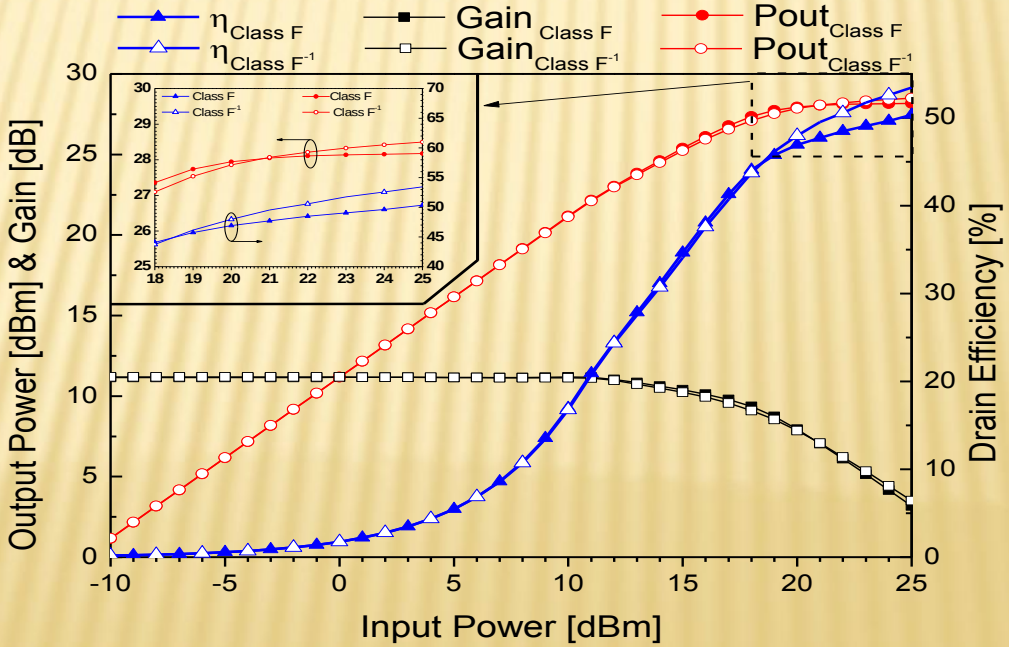


Class F^{-1} drain waveforms





GaAs FET
- f = 9.6GHz
- V_{DD}=8V
- V_{GG}=-0.35V
- 1 mm gate periph.



Class F PA
- Pout=28.1dBm
- η=50%

Class F^{-1} PA
- Pout=28.5dBm
- η=54%

CONCLUSIONS

- Efficiency in PA is a key aspect and can be improved at different design level
- Some methodologies to increase efficiency at circuit level have been revised
- Considering current mode PAs, the harmonic tuning approach has been introduced at a general level and different examples have been provided:
  - Class F PAs
  - ***2nd*** and ***2nd & 3rd*** Harmonic Tuned PAs
- Further amplifier modes have been described, still making use of the harmonic tuning theory:
  - Class J PA
  - Class F^{-1} PA

REFERENCES

1. Mishra, Umesh K.; Shen, L.; Kazior, T.E.; Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE , vol.96, no.2, pp.287,305, Feb. 2008 doi: 10.1109/JPROC.2007.911060
2. Runton, D.W.; Trabert, B.; Shealy, J.B.; Vetury, R., "History of GaN: High-Power RF Gallium Nitride (GaN) from Infancy to Manufacturable Process and Beyond," Microwave Magazine, IEEE , vol.14, no.3, pp.82,93
3. P. Colantonio, F. Giannini, and E. Limiti, High Efficiency RF and Microwave Solid State Power Amplifiers. United Kingdom: Wiley, 2009.
4. P. Colantonio, F. Giannini, R. Giofrè, E. Limiti, A. Serino M. Peroni, P. Romanini, C. Proietti "A C-Band High Efficiency Second Harmonic Tuned Hybrid Power Amplifier in GaN technology," IEEE Trans. on Microwave Th. and Tech., Vol. 54, n. 6-II, June 2006, pp. 2713-2722.
5. Grebennikov, A.V. (2000). Circuit design technique for high efficiency Class F amplifiers, IEEE MTT-S Int. Microwave Symp. Dig., Boston, MA, June 2000, Vol. 2, pp. 771–774.
6. S. Cripps, P. Tasker, A. Clarke, J. Lees, and J. Benedikt, "On the Continuity of High Efficiency Modes in Linear RF Power Amplifiers," Microwave and Wireless Components Letters, IEEE, vol. 19, no. 10, pp. 665 –667, oct. 2009.
7. P. Wright, J. Lees, J. Benedikt, P. Tasker, and S. Cripps, "A methodology for realizing high efficiency class-j in a linear and broadband pa," IEEE Trans. Microw. Theory Tech., vol. 57, no. 12, pp. 3196 – 3204, Dec. 2009.
8. E. Cipriani, P. Colantonio, F. Giannini, R. Giofré, "Theoretical and Experimental Comparisons of Class F vs. Class F-1 PAs" Proceedings of European Microwave Integrated Circuit Conference, EuMIC 2010, Paris, France.
9. E. Cipriani, P. Colantonio, F. Giannini, R. Giofré, "Effects of Gate Bias Voltage and Compression Level on a X-band MMIC Class F-1 PA", 6th European Microwave Integrated Circuit Conference, EuMIC 2011, Manchester, UK.
10. Goto, S.; Kunii, T.; Ohta, A.; Inoue, A.; Hosokawa, Y.; Hattori, R. & Mitsui, Y. (2001). Effect of Bias Condition and Input Harmonic Termination on High Efficiency Inverse Class-F Amplifiers, 31st European Microwave Conference, 2001. Oct. 2001, pp. 1 - 4.
11. Grebennikov, A. (2003). Switched-mode RF and microwave parallel-circuit Class E power amplifiers, Intern. Journal of RF and Microwave Computer-Aided Engineering, Vol. 14, No. 1, December 2003, pp. 21-35.
12. Grebennikov, A. & Sokal, N.O. (2007). Switchmode RF power amplifiers, Newnes, Elsevier, Burlington, MA, USA
13. Kazimierczuk M.K. (1981). Class E tuned power amplifier with shunt inductor, IEEE Journal of Solid-State Circuits, Vol. 16, No. 1, February 1981, pp. 2 – 7.
14. Kazimierczuk, M.K. (2008). RF Power Amplifiers, Wiley, New York.
15. Kazimierczuk M. K. & Jozwik, J. (1990). Analysis and design of class E zero-current switching rectifier, IEEE Trans. Circuits Syst., Vol. 37, No. 8, August 1990, pp. 1000- 1009.
16. E. Cipriani, P. Colantonio, F. Giannini and R. Giofré, "Theory and experimental validation of a Class E PA above theoretical maximum frequency", Int. Journal of Microwave and Wireless Technologies, Vol. 1, Sp. Is. 04, Aug. 2009, pp 293-299.

REFERENCES

17. Elisa Cipriani, Paolo Colantonio, Franco Giannini and Rocco Giofré (2010). The Switched Mode Power Amplifiers, Advanced Microwave and Milimeter Wave Technologies Semiconductor Devices Circuits and Systems, Moumita Mukherjee (Ed.), ISBN: 978-953-307-031-5, INTECH, Available from: http://sciyo.com/articles/show/title/the-switched-mode-power-amplifiers
18. E. Cipriani, P. Colantonio, F. Giannini, R. Giofrè, "Optimization of Class E Power Amplifier Design above Theoretical Maximum Frequency," Proceedings of the European Microwave Conference, EuMC 2008, Amsterdam, The Netherland, Oct. 2008, pp. 1541-1544.
19. Mader, T.B.; Bryerton, E.W.; Markovic, M.; Forman, M. & Popović, Z. (1998). Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array, IEEE Transactions on Microwave Theory and Techniques, Vol. 46, No. 10, Part 1, October 1998, pp. 1391 – 1398.
20. Mury, T. & Fusco, V.F. (2005). Series-L/parallel-tuned comparison with shunt-C/series tuned class-E power amplifier, IEE Proceedings Circuits, evices and Systems, December 2005, pp. 709 - 717.
21. Mury, T. & Fusco, V.F. (2007). Inverse Class-E Amplifier With Transmission-Line Harmonic Suppression, IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 54, No. 7, July 2007, pp. 1555 - 1561.